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Server/Workstation
Motherboard

TURIN2D24XGM/500W

User Manual

English

Version 1.00
Published May. 2026

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WARNING

THIS PRODUCT CONTAINS A BUTTON BATTERY
If swallowed, a button battery can cause serious injury or death.
Please keep batteries out of sight or reach of children

ASRock Rack's Website: www.ASRockRack.com

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

ASRock Rack INC. hereby declares that this device is in compliance with the essential requirements and other relevant provisions of related Directives. Full text of EU declaration of conformity is available at: http://www.asrockrack.com

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Please refer to https://www.asrockrack.com/general/about.asp?cat=Responsibility for information disclosure based on regulation requirements ASRock Rack is complied with.

ASRock Rack INC. hereby declares that this device is in compliance with the essential requirements and other relevant provisions of related UKCA Directives. Full text of UKCA declaration of conformity is available at: http://www.asrockrack.com

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Contents

Chapter 1 Introduction

Thank you for purchasing ASRock Rack ***TURIN2D24XGM/500W*** motherboard, a reliable motherboard produced under ASRock Rack's consistently stringent quality control. It delivers excellent performance with robust design conforming to ASRock Rack's commitment to quality and endurance.

In this manual, chapter 1 and 2 contains introduction of the motherboard and step-by-step guide to the hardware installation. Chapter 3 and 4 contains the configuration guide to BIOS setup and information of the software support.

Because the motherboard specifications and the BIOS software might be updated, the content of this manual will be subject to change without notice. In case any modifications of this manual occur, the updated version will be available on ASRock Rack website without further notice. Find the latest memory and CPU support lists on ASRock Rack website as well. ASRock Rack's Website: www.ASRockRack.com

Please visit the website for specific information and technical support: http://www.asrockrack.com/support/

1.1 Package Contents

- ASRock Rack TURIN2D24XGM/500W motherboard (MGX form factor: 424.5 mm x 305.59 mm)
- Quick installation guide
- 1 MCIO to x8 PCIe cable
- 2 Screws for M.2 sockets

If any items are missing or appear damaged, contact the authorized dealer.

English

1.2 Specifications

TURIN2D24XGM/500W	
Physical Status	
Form Factor	MGX
Dimension	16.7 in x 12 in (424.5 mm x 305.59 mm)
Processor System	
CPU	Supports AMD EPYC™ 9005 / 9004 (with AMD 3D V-Cache™ Technology) and 97x4 series processors
Socket	1+1 Socket SP5 (LGA 6096)
Chipset	System on Chip
System Memory	
Supported DIMM Quantity	12+12 DIMM slots (1DPC)
Supported Type	Supports DDR5 RDIMM, RDIMM-3DS
Max. Capacity per DIMM	RDIMM: 128 GB (2Rx4) RDIMM-3DS: 256 GB (2Rx4)
Max. DIMM Frequency	6400 MT/s
Voltage	1.1V
Note: Memory support is to be validated.	
PCIe Expansion Slots / Connectors	
M.2	1 M-key (PCIe 3.0 x4); supports 2280 form factor [CPU0] 1 M-key (PCIe 3.0 x4); supports 2280 form factor [CPU1]
MCIO	8 MCIO (PCIe 5.0 / CXL 2.0 x8) [CPU0] 2 MCIO (PCIe 5.0 x8) [CPU0] 8 MCIO (PCIe 5.0 / CXL 2.0 x8) [CPU1] 2 MCIO (PCIe 5.0 x8) [CPU1]
Ethernet	
Additional GbE Controller	2 RJ45 (1 GbE) by Intel® i350
Server Management	
BMC Controller	ASPEED AST2600 on DC-SCM 2.0 module (4UXGM_BMC)*
Dedicated IPMI LAN	1 Realtek RTL8211F for dedicated management LAN on 4UMGX_IOB*
**4UXGM_BMC and 4UMGX_IOB are additional cards.*	
I/O	
LAN Port	2 RJ45 (1 GbE) by Intel® i350
Internal Connectors/Headers	
Power Connector	4 Micro-fit (8-pin, ATX 12V), 1 Micro-fit (2-pin, 12VSB)
Auxiliary Panel Header	1 (18-pin): chassis intrusion, system fault LED, LAN activity LEDs, locate, SMBus
System Panel Header	1 (9-pin): power switch, reset switch, system power LED, HDD activity LED
NMI Header	1

Fan Header	2 (6-pin)
TPM Header	1 (13-pin, SPI)
HSBP	1
SMbus Header	4
IPMB Header	1
Clear CMOS	1 (contact pads)
Others	1 MGX_NCSI header, 2 MGX_FPB connectors, 1 RDS2 connector, 1 MGX_PDB header, 1 MGX_IOB header, 1 Rear Panel LAN LED header
LED Indicators	
Standby PWR LED	2 (3V)
80 Debug Port LED	1
Fan Fail LED	2
BMC Heartbeat LED	1 on DC-SCM 2.0 module (4UXGM_BMC*)
System Fault LED	1

**4UXGM_BMC is additional card.*

System BIOS	
Type	AMI UEFI BIOS: 256 Mb (32 MB) SPI Flash ROM
Features	ASRock Rack Instant Flash, ACPI 6.4 (and about) compliance wake-up events, SMBIOS 3.5.0 and above, Plug and Play (PnP)
Hardware Monitor	
Temperature	MB, I350 temperature sensing
Voltage	+12V, 5VSB, 12VSB, 3VSB, +3V, BAT, P0_VDD_18_DUAL, +1.8V
4UMGX_IOB, 4UMGX_FPB	
I/O	
UID Button w/LED	1 UID button w/ LED on 4UMGX_FPB 1 UID button on 4UMGX_IOB (back site)
Other Buttons	1 Power w/LED, 1 Reset and 1 NMI buttons on 4UMGX_FPB 1 Power button on 4UMGX_IOB (back site)
USB Port	3 Type-A (USB 3.2 Gen1): 1 on 4UMGX_IOB 2 on 4UMGX_FPB
LAN Port	2 RJ45 (1 GbE) on 4UMGX_IOB 1 dedicated IPMI on 4UMGX_IOB
Video Port	1 Mini-DP on 4UMGX_IOB
LED Indicators	
System Fault LED	1 on 4UMGX_IOB and 1 on 4UMGX_FPB
LAN LED	2 on 4UMGX_FPB

HDD LED	1 on 4UMGX_FPB
Support OS	
OS	Microsoft® Windows: (for EPYC 9004) - Server 2019 (64 bit) - Server 2022 (64 bit) Microsoft® Windows: (for EPYC 9005) - Server 2019 (64 bit) - Server 2022 (64 bit) - Server 2025 (64 bit) Linux: (for EPYC 9004) - RedHat Enterprise Linux Server 8.6 (64 bit) / Server 8.7 (64 bit) / Server 9.0 (64 bit) / Server 9.1 (64 bit) - SUSE SLES 15.4 (64 bit) - UBuntu 20.04.5 (64 bit) / 22.04 (64 bit) / 22.10 (64 bit) Linux: (for EPYC 9005) - RedHat Enterprise Linux Server 8.10 (64 bit) / Server 9.4 (64 bit) - SUSE SLES 15.6 (64 bit) - UBuntu 22.04.5 (64 bit) / 24.04.2 (64 bit) Hypervisor: (for EPYC 9004) - VMWare® ESXi 8.0 Hypervisor: (for EPYC 9005) - VMWare® ESXi 9.0 ** Please refer to the website for the latest OS support list.*
Environment	
Temperature	Operating temperature: 10°C ~ 35°C Non-operating temperature: -40°C ~ 70°C
Humidity	Non-operating humidity: 20% ~ 90% (non-condensing)

Note: Please refer to the website for the latest specifications.

This motherboard supports Wake from on Board LAN. To use this function, please make sure that the "Wake on Magic Packet from power off state" is enabled in Device Manager > Intel® Ethernet Connection > Power Management. And the "PCI Devices Power On" is enabled in UEFI SETUP UTILITY > Advanced > ACPI Configuration. After that, onboard LAN1&2 can wake up S5 under OS.

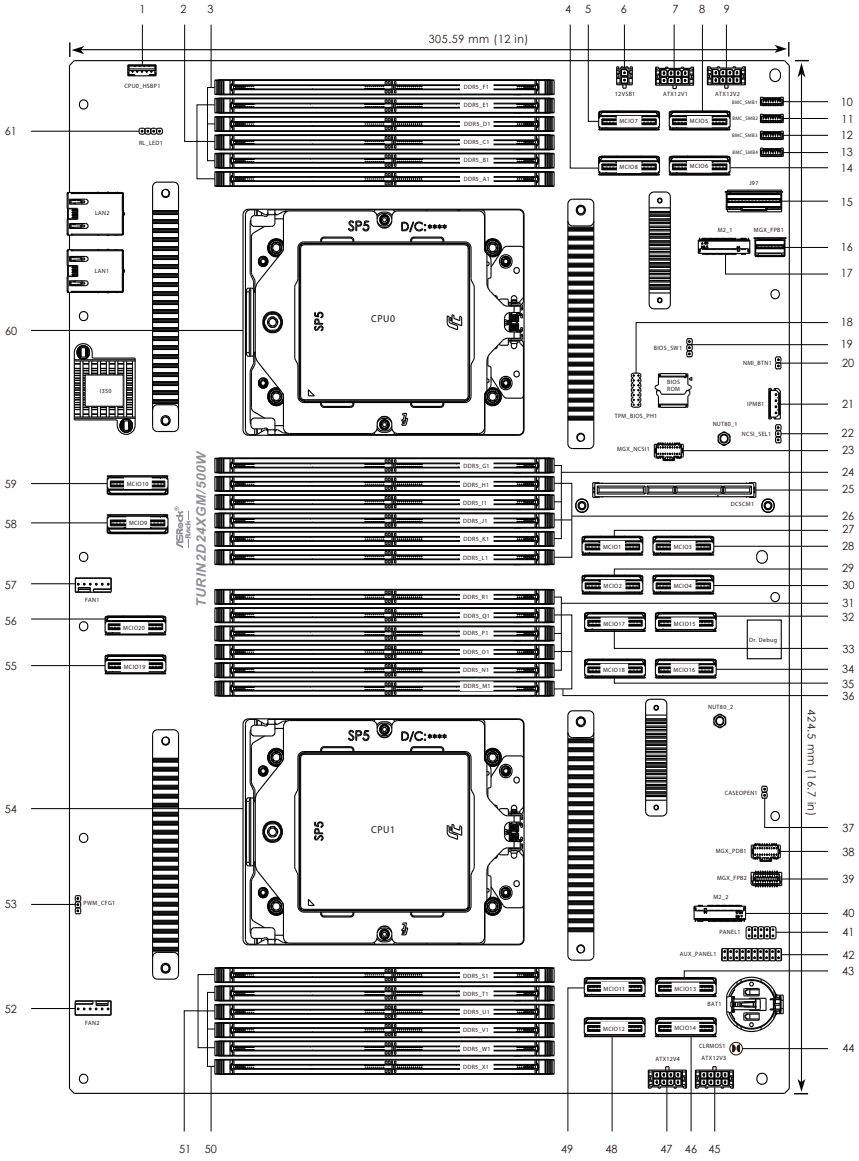
If installing Intel® LAN utility or Marvell SATA utility, this motherboard may fail Windows® Hardware Quality Lab (WHQL) certification tests. If installing the drivers only, it will pass the WHQL tests.

English

1.3 Unique Features

ASRock Rack Instant Flash is a BIOS flash utility embedded in Flash ROM. This convenient BIOS update tool allows user to update system BIOS without entering operating systems first like MS-DOS or Windows®. With this utility, press the <F6> key during the POST or the <F2> key to enter into the BIOS setup menu to access ASRock Rack Instant Flash. Just launch this tool and save the new BIOS file to the USB flash drive, floppy disk or hard drive, then update the BIOS only in a few clicks without preparing an additional floppy diskette or other complicated flash utility. Please be noted that the USB flash drive or hard drive must use FAT32/16/12 file system.

1.4 Motherboard Layout



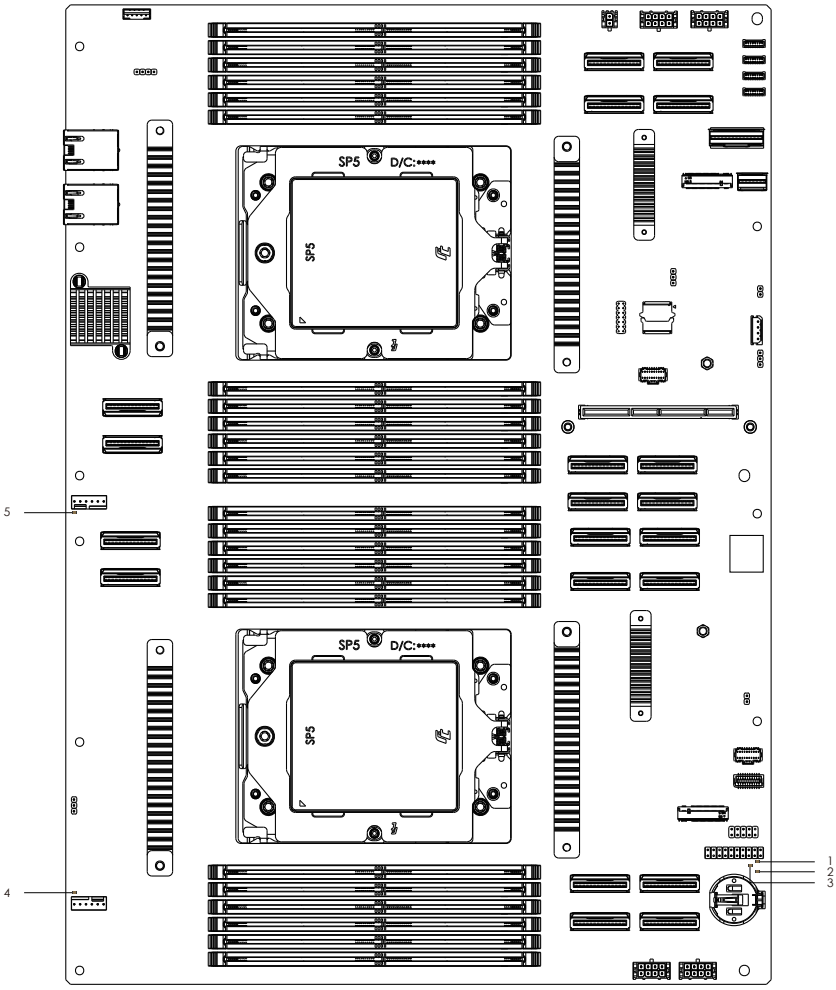
The illustration here is for references only. The actual layout may slightly vary depending on the model and the version used.

No.	Description
1	Backplane PCI Express Hot-Plug Connector (CPU0_HSBP1)
2	3 DDR5 DIMM Slots (DDR5_A1, DDR5_C1, DDR5_E1)*
3	3 DDR5 DIMM Slots (DDR5_B1, DDR5_D1, DDR5_F1)*
4	Mini Cool Edge IO Connector (MCIO8)
5	Mini Cool Edge IO Connector (MCIO7)
6	12V Micro-fit Power Connector (12VSB1)
7	ATX 12V Power Connector (ATX12V1)
8	Mini Cool Edge IO Connector (MCIO5)
9	ATX 12V Power Connector (ATX12V2)
10	BMC SMBus Header (BMC_SMB1)
11	BMC SMBus Header (BMC_SMB2)
12	BMC SMBus Header (BMC_SMB3)
13	BMC SMBus Header (BMC_SMB4)
14	Mini Cool Edge IO Connector (MCIO6)
15	I/O Card Connector (J97)
16	Front Panel Board Connector (MGX_FPB1)
17	M.2 Socket (M2_1) (Type 2280)
18	SPI TPM Header (TPM_BIOS_PH1)
19	BIOS Selection Jumper (BIOS_SW1)
20	Non Maskable Interrupt Button (NMI_BTN1)
21	Intelligent Platform Management Bus Header (IPMB1)
22	NCSI Mode Jumper (NCSI_SEL1)
23	Network Controller Sideband Interface Header (MGX_NCSI1)
24	3 DDR5 DIMM Slots (DDR5_G1, DDR5_I1, DDR5_K1)*
25	Datacenter-ready Secure Control Module Slot (DCSCM1)
26	3 DDR5 DIMM Slots (DDR5_H1, DDR5_J1, DDR5_L1)*
27	Mini Cool Edge IO Connector (MCIO1)
28	Mini Cool Edge IO Connector (MCIO3)
29	Mini Cool Edge IO Connector (MCIO2)
30	Mini Cool Edge IO Connector (MCIO4)
31	3 DDR5 DIMM Slots (DDR5_N1, DDR5_P1, DDR5_R1)*
32	Mini Cool Edge IO Connector (MCIO15)
33	Mini Cool Edge IO Connector (MCIO17)
34	Mini Cool Edge IO Connector (MCIO16)

No.	Description
35	Mini Cool Edge IO Connector (MCIO18)
36	3 DDR5 DIMM Slots (DDR5_M1, DDR5_O1, DDR5_Q1)*
37	Chassis Intrusion Header (CASEOPEN_1)
38	Power Distribution Board Header (MGX_PDB1)
39	Front Panel Board Connector (MGX_FPB2)
40	M.2 Socket (M2_2) (Type 2280)
41	System Panel Header (PANEL1)
42	Auxiliary Panel Header (AUX_PANEL1)
43	Mini Cool Edge IO Connector (MCIO13)
44	Clear CMOS Pad (CLRMOS1)
45	ATX 12V Power Connector (ATX12V3)
46	Mini Cool Edge IO Connector (MCIO14)
47	ATX 12V Power Connector (ATX12V4)
48	Mini Cool Edge IO Connector (MCIO12)
49	Mini Cool Edge IO Connector (MCIO11)
50	3 DDR5 DIMM Slots (DDR5_T1, DDR5_V1, DDR5_X1)*
51	3 DDR5 DIMM Slots (DDR5_S1, DDR5_U1, DDR5_W1)*
52	System Fan Header (FAN2)
53	PWM Configuration Header (PWM_CFG1)
54	Socket SP5 (LGA 6096) (CPU1)
55	Mini Cool Edge IO Connector (MCIO19)
56	Mini Cool Edge IO Connector (MCIO20)
57	System Fan Header (FAN1)
58	Mini Cool Edge IO Connector (MCIO9)
59	Mini Cool Edge IO Connector (MCIO10)
60	Socket SP5 (LGA 6096) (CPU0)
61	Rear Panel LAN LED (RL_LED)

**For DIMM installation and configuration instructions, please see p.18 (Installing the Memory Modules (DIMM)) for more details.*

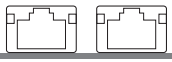
1.5 Onboard LED Indicators



No.	Item	Status	Description
1	SYS_LED1	Red	System failed
2	SB_PWR1	Green	STB PWR ready
3	SB_PWR2	Green	STB PWR ready
4	LED_FAN2	Red	FAN2 failed
5	LED_FAN1	Red	FAN1 failed

English

1.6 I/O Panel



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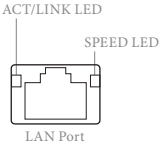
No.	Description
1	1G LAN RJ-45 Port (LAN2)*
2	1G LAN RJ-45 Port (LAN1, shared NIC)*

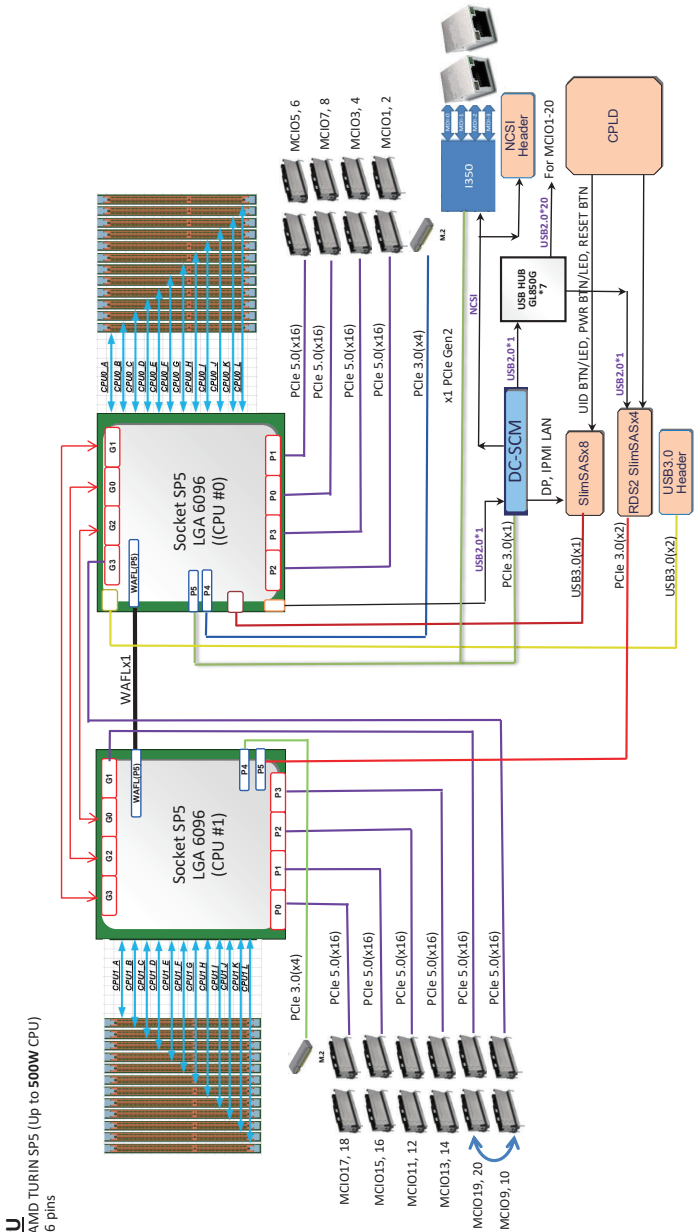
*There are two LEDs on the 1G LAN port specified for link activity and speed. Please refer to the table below for the LAN port LED indications.



1G LAN Port (LAN1, LAN2) LED Indications

Activity / Link LED		Speed LED	
Status	Description	Status	Description
Off	No link	Off	10 Mbps connection or no link
Blinking Orange	Data activity	Orange	100 Mbps connection
On	Link	Green	1 Gbps connection

1.7 Block Diagram



English

Chapter 2 Installation

This is a MGX form factor 424.5 mm x 305.59 mm motherboard. Before installing the motherboard, study the configuration of the chassis to ensure that the motherboard fits into it.

1. *Ensure the motherboard battery is installed before unplugging the power cord or installing/removing the motherboard.*
2. *Before installing or removing any component, ensure that the power supply is off or the power cord is detached from the power supply. Failure to do so may cause severe damage to the motherboard, peripherals, and/or components.*

2.1 Screw Holes

Place screws into the holes indicated by circles to secure the motherboard to the chassis.

Do not over-tighten the screws! Doing so may damage the motherboard.

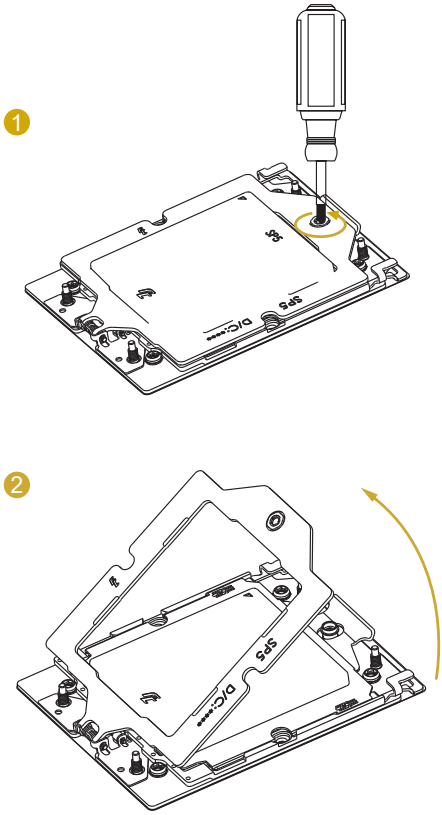
2.2 Pre-installation Precautions

Take note of the following precautions before installing motherboard components or change any motherboard settings.

1. Unplug the power cord from the wall socket before touching any components.
2. To avoid damaging the motherboard's components due to static electricity, NEVER place the motherboard directly on the carpet or the like. Also remember to use a grounded wrist strap or touch a safety grounded object before handling the components.
3. Hold components by the edges and do not touch the ICs.
4. Whenever uninstall any component, place it on a grounded anti-static pad or in the bag that comes with the component.
5. When placing screws into the screw holes to secure the motherboard to the chassis, please do not over-tighten the screws! Doing so may damage the motherboard.

2.3 Installing the CPU

1. *Before inserting the CPU into the socket, please check if the PnP cap is on the socket, if the CPU surface is unclean, or if there are any bent pins in the socket. Do not force to insert the CPU into the socket if above situation is found. Otherwise, the CPU will be seriously damaged.*
2. *Unplug all power cables before installing the CPU.*



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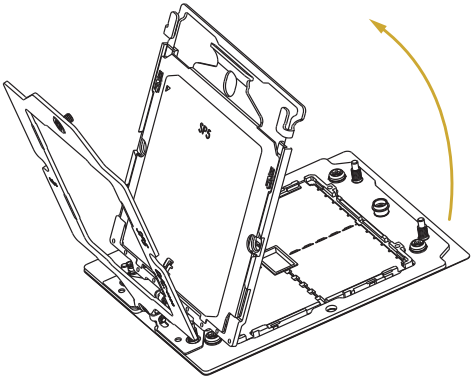

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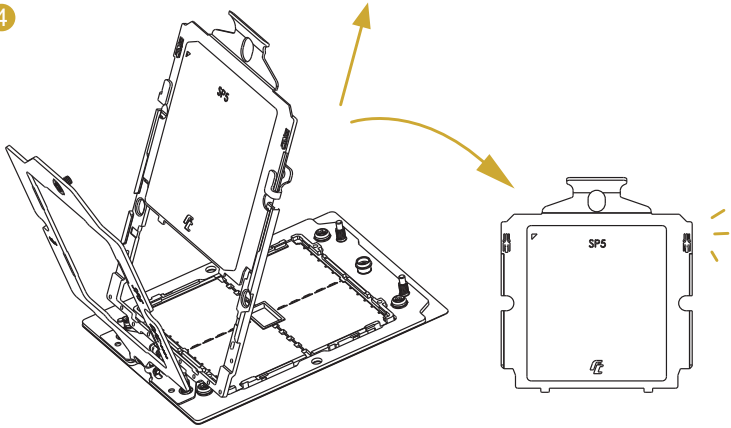

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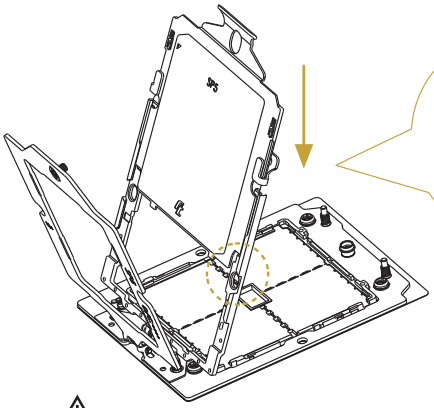
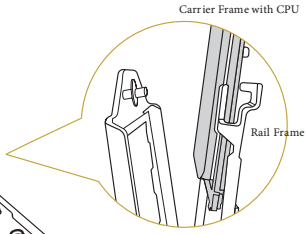
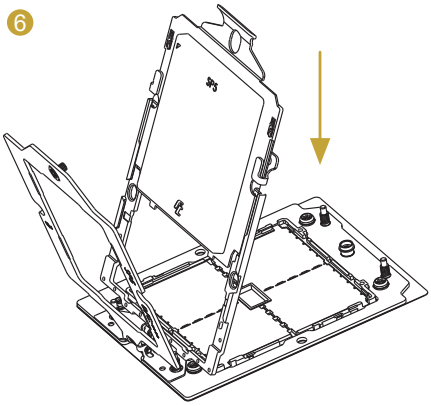




Please make sure that the carrier frame with CPU is closely attached to the rail frame while inserting it.

⚠ Install the carrier frame with CPU. Don't separate them.

6



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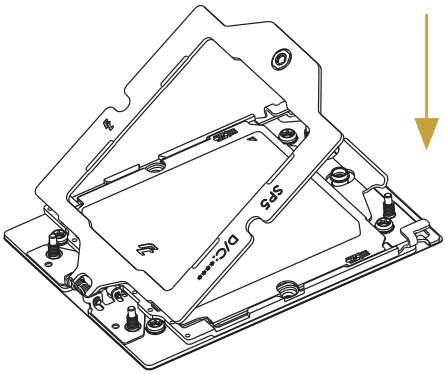

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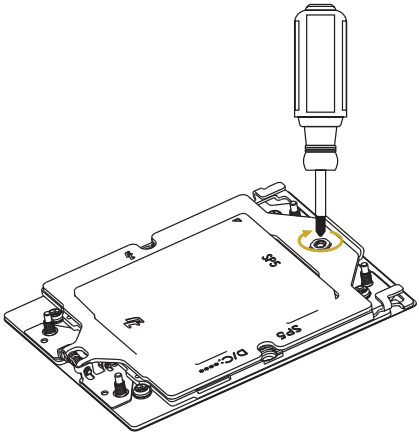

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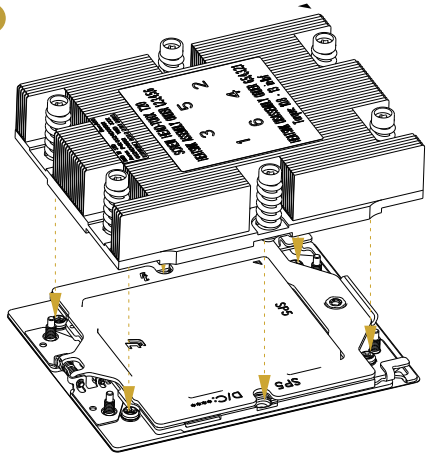

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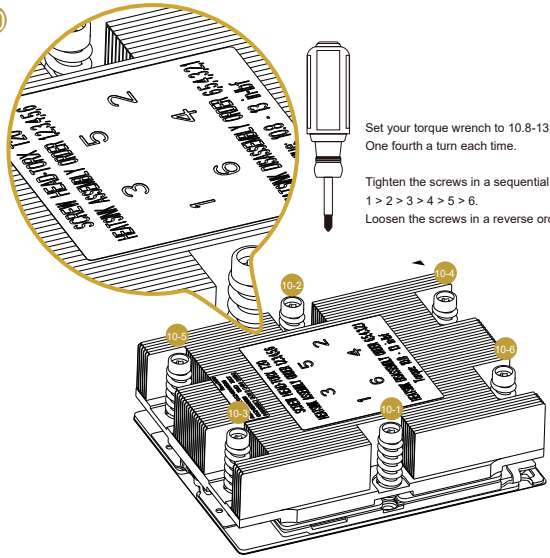


Set your torque wrench to 10.8-13.0 in-lb.
One fourth a turn each time.

Tighten the screws in a sequential order
1 > 2 > 3 > 4 > 5 > 6.
Loosen the screws in a reverse order.

2.4 Installing the Memory Modules (DIMM)

This motherboard provides twenty-four DDR5 (Double Data Rate 5) DIMM slots in two groups, and supports Single Channel Memory Technology.

CPU0	CPU1
DDR5_A1, B1, C1, D1, E1, F1	DDR5_M1, N1, O1, P1, Q1, R1
DDR5_G1, H1, I1, J1, K1, L1	DDR5_S1, T1, U1, V1, W1, X1

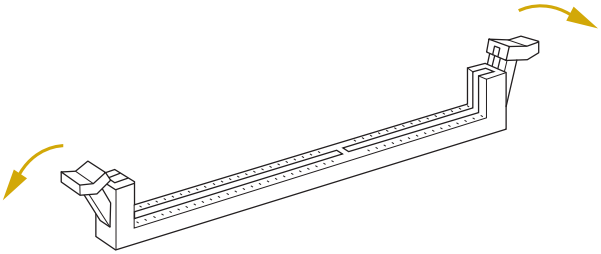
1. *It is not allowed to install a DDR, DDR2, DDR3 or DDR4 memory module into a DDR5 slot; otherwise, this motherboard and DIMM may be damaged.*
2. *For single channel configuration, it always needs to install identical (the same brand, speed, size and chip-type) DDR5 DIMMs.*

Recommended Memory Configurations

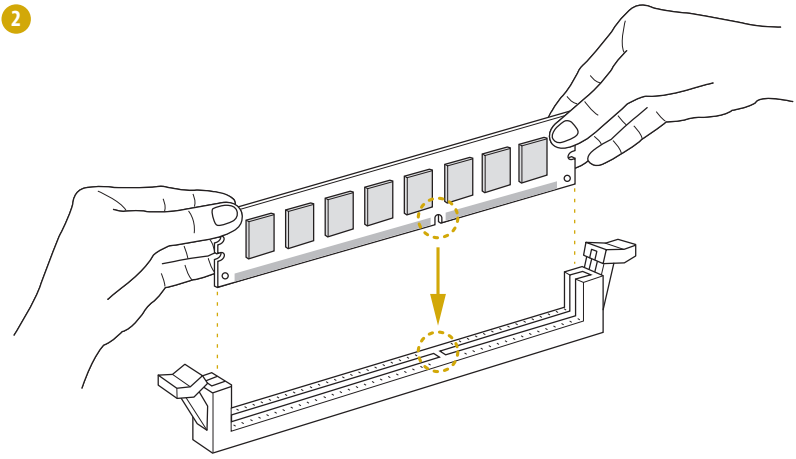
Number of Memory Channels Populated	Number of CPU Installed	AMD Recommended Memory Channels																								
		CPU0													CPU1											
		A1	B1	C1	D1	E1	F1	G1	H1	I1	J1	K1	L1	M1	N1	O1	P1	Q1	R1	S1	T1	U1	V1	W1	X1
24	2P	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	1P																								
20	2P	V	V	V	V	V		V	V	V	V	V		V	V	V	V	V		V	V	V	V	V	
	1P																								
16	2P	V	V	V		V		V	V	V		V		V	V	V		V		V	V	V		V	
	1P																								
12	2P	V	V	V				V	V	V				V	V	V				V	V	V			
	1P	V	V	V	V	V	V	V	V	V	V	V	V												
10	2P																								
	1P	V	V	V	V	V		V	V	V	V	V													
8	2P	V		V				V		V				V		V				V		V			
	1P	V	V	V		V		V	V	V		V													
6	2P																								
	1P	V	V	V				V	V	V															
4	2P	V						V		V				V						V					
	1P	V		V				V		V															
2	2P	V												V											
	1P	V						V																	
1	2P																								
	1P	V																							

The symbol V indicates the slot is populated.

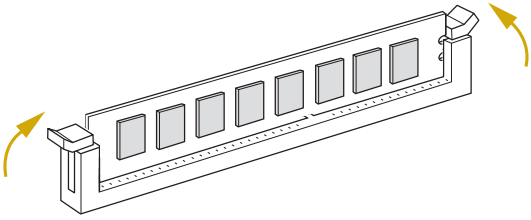
1



2



3



English

2.5 Expansion Slot

There is one expansion slot on this motherboard for BMC card connections.

Expansion slot:

DCSCM1 is used for BMC card (4UXGM_BMC) connection.

Installing an expansion card

Step 1. Before installing an expansion card, please make sure that the power supply is switched off or the power cord is unplugged. Please read the documentation of the expansion card and make necessary hardware settings for the card before starting the installation.

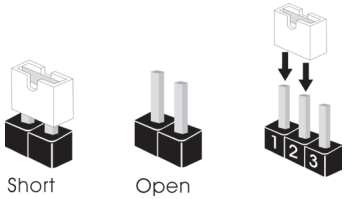
Step 2. Remove the system unit cover (if the motherboard is already installed in a chassis).

Step 3. Align the card connector with the slot and press firmly until the card is completely seated on the slot.

Step 4. Replace the system cover.

2.6 Jumper Setup

The illustration shows how jumpers are setup. When the jumper cap is placed on the pins, the jumper is “Short”. If no jumper cap is placed on the pins, the jumper is “Open”. The illustration shows a 3-pin jumper whose pin1 and pin2 are “Short” when a jumper cap is placed on these 2 pins.



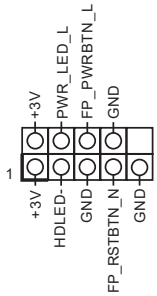
NCSI Mode Jumper (3-pin NCSI_SEL1) (see p.6, No. 22)	 NCSI to I350 (Default)	 NCSI to NCSI Header
BIOS Selection Jumper (3-pin BIOS_SW1) (see p.6, No. 19)	 SPI to on board BIOS SKT (Default)	 SPI to DCSCM

English

2.7 Onboard Headers and Connectors

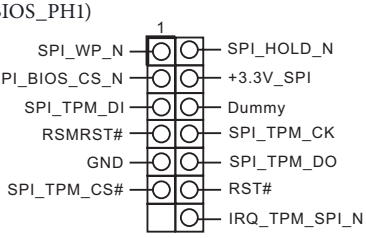
Onboard headers and connectors are NOT jumpers. Do NOT place jumper caps over these headers and connectors. Placing jumper caps over the headers and connectors will cause permanent damage to the motherboard.

System Panel Header
(9-pin PANEL1)
(see p.6, No.41)



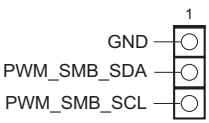
Connect the power switch, reset switch and system status indicator on the chassis to this header according to the pin assignments. Particularly note the positive and negative pins before connecting the cables.

SPI TPM Header
(13-pin TPM_BIOS_PH1)
(see p.6, No.18)



This connector supports SPI Trusted Platform Module (TPM) system, which can securely store keys, digital certificates, passwords, and data. A TPM system also helps enhance network security, protects digital identities, and ensures platform integrity.

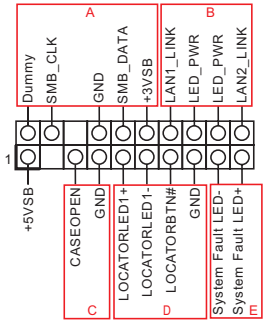
PWM Configuration
Header
(3-pin PWM_CFG1)
(see p.6, No.53)



This header is used for PWM configurations.

English

Auxiliary Panel Header
(18-pin AUX_PANEL1)
(see p.6, No.42)



This header supports multiple functions on the front panel, including the front panel SMB, internet status indicator and chassis intrusion pin.

A. Front panel SMBus connecting pin (6-1 pin FPSMB):
This header allows user to connect SMBus (System Management Bus) equipment. It can be used for communication between peripheral equipment in the system, which has slower transmission rates, and power management equipment.

B. Internet status indicator (4-pin LAN1, LAN2, LEDs):
This header allows user to use the Gigabit internet indicator cable to connect to the LAN status indicator. When this indicator flickers, it means that the internet is properly connected.

C. Chassis intrusion pin (2-pin CHASSIS):
This header is provided for host computer chassis with chassis intrusion detection designs. In addition, it must also work with external detection equipment, such as a chassis intrusion detection sensor or a microswitch. When this function is activated, if any chassis component movement occurs, the sensor will immediately detect it and send a signal to this header, and the system will then record this chassis intrusion event. The default setting is set to the CASEOPEN and GND pin; this function is off.

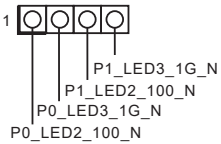
D. Locator LED (4-pin LOCATOR):
This header is for the locator switch and LED on the front panel.

E. System Fault LED (2-pin SYSTEM STATUS):
This header is for the Fault LED on the system.

Non Maskable Interrupt
Button Header
(NMI_BTN1)
(see p.6, No.40)

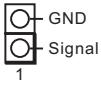
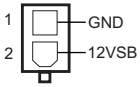
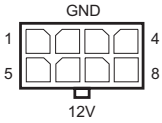
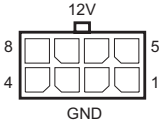
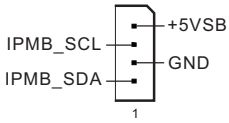
Please connect a NMI device to this header.

Rear Panel LAN LED
Header
(4-pin RL_LED)
(see p.6, No. 50)



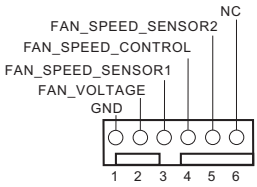
This header is used for extended LAN LED on the rear panel of a server system.

English

Chassis Intrusion Header (2-pin CASEOPEN1) (see p.6, No. 37)		This motherboard supports CASE OPEN detection feature that detects if the chassis cover has been removed. This feature requires a chassis with chassis intrusion detection design.
12V Micro-fit Power Connector (2-pin 12VSB1) (see p.6, No. 6)		This motherboard provides a 2-pin Micro-fit 12V power connector.
ATX 12V Power Connectors (8-pin ATX12V1) (see p.6, No.7) (8-pin ATX12V2) (see p.6, No.9)		This motherboard provides four 8-pin ATX 12V power connectors.
(8-pin ATX12V3) (see p.6, No.45) (8-pin ATX12V4 (see p.6, No.47)		
Intelligent Platform Management Bus header (4-pin IPMB1) (see p.6, No.21)		This 4-pin connector is used to provide a cabled base-board or front panel connection for value added features and 3rd-party add-in cards, such as Emergency Management cards, that provide management features using the IPMB.

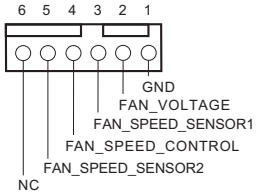
English

System Fan Headers
(6-pin FAN1)
(see p.6, No.57)

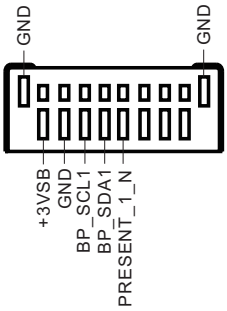


Please connect fan cables to the fan headers and match the black wire to the ground pin. All fans support fan control. The fan max. current is 5A and the max. power is 60Watts.

(6-pin FAN2)
(see p.6, No.52)

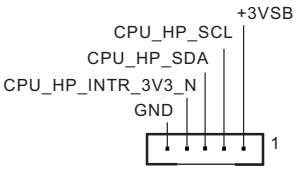


BMC SMBus Headers
(16-pin BMC_SMB1)
(see p.6, No.10)
(16-pin BMC_SMB2)
(see p.6, No.11)
(16-pin BMC_SMB3)
(see p.6, No.12)
(16-pin BMC_SMB4)
(see p.6, No.13)



These headers are used for the SM BUS devices.

Backplane PCI Express
Hot-Plug Connectors
(5-pin CPU0_HSBP1)
(see p.6, No.1)



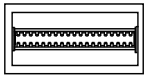
This header is used for the hot plug feature of HDDs on the backplane.

Clear CMOS Pad
(CLRMOS1)
(see p.6, No.44)

CLRMOS1 allows user to clear the data in CMOS. To clear CMOS, take out the CMOS battery and short the Clear CMOS Pad.

English

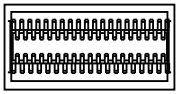
Front Panel Board Connector (20-pin MGX_FPB2) (see p.6, No.39)



Connect this to the 4UMGX_FPB to configure the power button, reset, UID and system fault LED features.

Pin	Defeinition	Pin	Defeinition
1	PWR_BTN_THRUIN_N	2	P3V3_STBY
3	RST_BTN_THRUIN_N	4	+5V_AUX
5	LOCATORBTN#_H	6	+5V_AUX
7	PWR_LED_L	8	GND
9	LOCATORLED-	10	GND
11	SYSTEM_FAULT_LED_N	12	GND
13	FFU1_LED_L	14	SMB_BMC_STBY_LVC3_SCL
15	FFU2_LED_L	16	SMB_BMC_STBY_LVC3_SDA
17	FFU3_LED_L	18	SNN_FFU1
19	FFU4_LED_L	20	SNN_FFU2

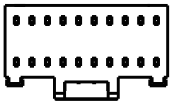
Front Panel Board Connector (38-pin MGX_FPB1) (see p.6, No.16)



Connect this to the 4UMGX_FPB to provide USB signal.

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	FRONT_USB3_RX_DP1	B2	FRONT_USB3_RX_DP2
A3	FRONT_USB3_RX_DN1	B3	FRONT_USB3_RX_DN2
A4	GND	B4	GND
A5	FRONT_USB3_TX_DP1	B5	FRONT_USB3_TX_DP2
A6	FRONT_USB3_TX_DN1	B6	FRONT_USB3_TX_DN2
A7	GND	B7	GND
A8	P5V_USB_FP_P1	B8	P5V_USB_FP_P2
A9	P5V_USB_FP_P1	B9	P5V_USB_FP_P2
A10	GND	B10	DP_HPD_J87
A11	DP_AUX_J87_P	B11	+3VSB
A12	DP_AUX_J87_N	B12	DP_MUX_SEL
A13	GND	B13	GND
A14	DP_TXD0_J87_P	B14	DP_TXD1_J87_P
A15	DP_TXD0_J87_N	B15	DP_TXD1_J87_N
A16	GND	B16	GND
A17	USB2_FRONT_R_DP1	B17	USB2_FRONT_R_DP2
A18	USB2_FRONT_R_DN1	B18	USB2_FRONT_R_DN2
A19	GND	B19	GND

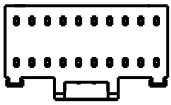
Network Controller Side-band Interface Header (20-pin MGX_NCSI1) (see p.6, No.23)



This header is used for providing NCSI signal to the system.

Pin	Defeinition	Pin	Defeinition
1	GND	2	PKG_ID1
3	NCSI_RX_D0	4	CLK_50M_NCSI
5	NCSI_RX_D1	6	GND
7	NCSI_CRS_DV	8	ISOLATE_N
9	GND	10	PKG_ID0
11	NCSI_TX_EN	12	GND
13	NCSI_TX_D0	14	UART5_BMC_TX
15	NCSI_TX_D1	16	UART5_BMC_RX
17	AOC_NCSI_PRSNT_N_R	18	GND
19	NC_ARB_OUT	20	NC_ARB_IN

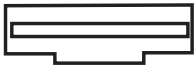
Power Distribution Board Header (20-pin MGX_PDB1) (see p.6, No.38)



Connect this header to 4UMGX_PDB for providing power signal.

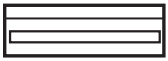
Pin	Defeinition	Pin	Defeinition
1	PRSNT1_L	2	PRSNT2_L
3	PRSNT3_L	4	PRSNT4_L
5	PWOK1	6	PWOK2
7	PWOK3	8	PWOK4
9	PSON#	10	SMB_BMC_STBY_LVC3_ALT
11	PSU_VIN_GOOD1	12	SMB_BMC_STBY_LVC3_SDA
13	-	14	SMB_BMC_STBY_LVC3_SCL
15	-	16	GND
17	-	18	P12V_PSU0_SENSE_P
19	-	20	P12V_PSU0_SENSE_N

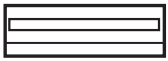
I/O Connector
(J97)
(see p.6, No.15)



This connector is used for 4UMGX_IOB connection.

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	HSO0_BMC_RTL_RX_P	B2	HSI0_BMC_RTL_TX_P
A3	HSO0_BMC_RTL_RX_N	B3	HSI0_BMC_RTL_TX_N
A4	GND	B4	GND
A5	DP_TXD0_P	B5	DP_TXD1_P
A6	DP_TXD0_N	B6	DP_TXD1_N
A7	GND	B7	GND
A8	PWR_BTN_N	B8	FFU_UART_TX
A9	PWR_LED_L	B9	FFU_UART_RX
A10	RST_BTN_N	B10	RSVD
A11	LOCATORBTN#_H	B11	UART0_TX_BMC_3V3
A12	LOCATORLED-	B12	UART0_RX_BMC_3V3
A13	GND	B13	GND
A14	IOB_PERST_N	B14	NCSI_CRS_DV
A15	IOB_WAKE_N	B15	NCSI_TX_EN
A16	GND	B16	GND
A17	GREEN_LINK_L_LED	B17	AMBER_LINK_L_LED
A18	NCSI_RX_D1	B18	AMBER_FAULT_L_LED
A19	GND	B19	GND
A20	RSVD	B20	NCSI_CLK
A21	RSVD	B21	IOB_PRSNT_N
A22	GND	B22	GND
A23	REFCLK_DP2	B23	IOB_IOEXP_INT_L
A24	REFCLK_DN2	B24	DP_HPD
A25	GND	B25	GND
A26	1SMB_BMC_STBY_LVC3_SCL	B26	USB_OC_N
A27	SMB_BMC_STBY_LVC3_SDA	B27	REAR_USB_EN
A28	MB_PRSNT_N	B28	PHY_RST_N
A29	BMC_SMBCLK5	B29	PHY_MDC_R
A30	BMC_SMBDATA5	B30	PHY_MDIO_R
A31	GND	B31	GND
A32	DP_AUX_P	B32	R_DP1
A33	DP_AUX_N	B33	R_DM1
A34	GND	B34	GND
A35	USB3_HUB_RXP1	B35	USB3_HUB_TXP1
A36	USB3_HUB_RXN1	B36	USB3_HUB_TXN1
A37	GND	B37	GND

MCIO Connectors (MCIO1) (see p.6, No.27) (MCIO2) (see p.6, No.29) (MCIO3) (see p.6, No.28) (MCIO4) (see p.6, No.30) (MCIO5) (see p.6, No.8) (MCIO6) (see p.6, No.14) (MCIO7) (see p.6, No.5) (MCIO8) (see p.6, No.4) (MCIO11) (see p.6, No.49) (MCIO12) (see p.6, No.48) (MCIO13) (see p.6, No.43) (MCIO14) (see p.6, No.46) (MCIO15) (see p.6, No.32) (MCIO16) (see p.6, No.34) (MCIO17) (see p.6, No.33) (MCIO18) (see p.6, No.35) (MCIO19) (see p.6, No.55) (MCIO20) (see p.6, No.56)		These connectors are used for the PCIE devices.

(MCIO9) (see p.6, No.58) (MCIO10) (see p.6, No.59)		These connectors are used for the PCIE devices.

MCIO1 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P2_RX_DP7	B2	P2_TX_DN7
A3	P2_RX_DN7	B3	P2_TX_DP7
A4	GND	B4	GND
A5	P2_RX_DP6	B5	P2_TX_DN6
A6	P2_RX_DN6	B6	P2_TX_DP6
A7	GND	B7	GND
A8	MCIO1_1_BP_TYPE	B8	SMB_MCIO1_SCL1
A9	MCIO1_1_WAKE#	B9	SMB_MCIO1_SDA1
A10	GND	B10	GND
A11	CLK_MCIO1_DP1	B11	MCIO1_PERST_BUF1_N
A12	CLK_MCIO1_DN1	B12	MCIO1_1_PRSNT_N
A13	GND	B13	GND
A14	P2_RX_DP5	B14	P2_TX_DN5
A15	P2_RX_DN5	B15	P2_TX_DP5
A16	GND	B16	GND
A17	P2_RX_DP4	B17	P2_TX_DN4
A18	P2_RX_DN4	B18	P2_TX_DP4
A19	GND	B19	GND
A20	P2_RX_DP3	B20	P2_TX_DN3
A21	P2_RX_DN3	B21	P2_TX_DP3
A22	GND	B22	GND
A23	P2_RX_DP2	B23	P2_TX_DN2
A24	P2_RX_DN2	B24	P2_TX_DP2
A25	GND	B25	GND
A26	SMB_MCIO1_SDA2	B26	MCIO1_2_BP_TYPE
A27	SMB_MCIO1_SCL2	B27	MCIO1_2_WAKE#
A28	GND	B28	GND
A29	MCIO1_USB2_P	B29	MCIO1_PERST_BUF2_N
A30	MCIO1_USB2_N	B30	MCIO1_CLKREQ
A31	GND	B31	GND
A32	P2_RX_DP1	B32	P2_TX_DN1
A33	P2_RX_DN1	B33	P2_TX_DP1
A34	GND	B34	GND
A35	P2_RX_DP0	B35	P2_TX_DN0
A36	P2_RX_DN0	B36	P2_TX_DP0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO2 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P2_RX_DN15	B2	P2_TX_DP15
A3	P2_RX_DP15	B3	P2_TX_DN15
A4	GND	B4	GND
A5	P2_RX_DP14	B5	P2_TX_DN14
A6	P2_RX_DN14	B6	P2_TX_DP14
A7	GND	B7	GND
A8	MCIO2_1_BP_TYPE	B8	SMB_MCIO2_SCL1
A9	MCIO2_1_WAKE#	B9	SMB_MCIO2_SDA1
A10	GND	B10	GND
A11	CLK_MCIO2_DP1	B11	MCIO2_PERST_BUF1_N
A12	CLK_MCIO2_DN1	B12	MCIO2_1_PRSNT_N
A13	GND	B13	GND
A14	P2_RX_DP13	B14	P2_TX_DN13
A15	P2_RX_DN13	B15	P2_TX_DP13
A16	GND	B16	GND
A17	P2_RX_DP12	B17	P2_TX_DN12
A18	P2_RX_DN12	B18	P2_TX_DP12
A19	GND	B19	GND
A20	P2_RX_DP11	B20	P2_TX_DN11
A21	P2_RX_DN11	B21	P2_TX_DP11
A22	GND	B22	GND
A23	P2_RX_DP10	B23	P2_TX_DN10
A24	P2_RX_DN10	B24	P2_TX_DP10
A25	GND	B25	GND
A26	SMB_MCIO2_SDA2	B26	MCIO2_2_BP_TYPE
A27	SMB_MCIO2_SCL2	B27	MCIO2_2_WAKE#
A28	GND	B28	GND
A29	MCIO2_USB2_P	B29	MCIO2_PERST_BUF2_N
A30	MCIO2_USB2_N	B30	MCIO2_CLKREQ
A31	GND	B31	GND
A32	P2_RX_DP9	B32	P2_TX_DN9
A33	P2_RX_DN9	B33	P2_TX_DP9
A34	GND	B34	GND
A35	P2_RX_DP8	B35	P2_TX_DN8
A36	P2_RX_DN8	B36	P2_TX_DP8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO3 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P3_RX_DP7	B2	P3_TX_DP7
A3	P3_RX_DN7	B3	P3_TX_DN7
A4	GND	B4	GND
A5	P3_RX_DP6	B5	P3_TX_DN6
A6	P3_RX_DN6	B6	P3_TX_DP6
A7	GND	B7	GND
A8	MCIO3_1_BP_TYPE	B8	SMB_MCIO3_SCL1
A9	MCIO3_1_WAKE#	B9	SMB_MCIO3_SDA1
A10	GND	B10	GND
A11	CLK_MCIO3_DP1	B11	MCIO3_PERST_BUF1_N
A12	CLK_MCIO3_DN1	B12	MCIO3_1_PRSNT_N
A13	GND	B13	GND
A14	P3_RX_DP5	B14	P3_TX_DN5
A15	P3_RX_DN5	B15	P3_TX_DP5
A16	GND	B16	GND
A17	PE0_RX_DP4	B17	P3_TX_DN4
A18	PE0_RX_DN4	B18	P3_TX_DP4
A19	GND	B19	GND
A20	P3_RX_DP3	B20	P3_TX_DN3
A21	P3_RX_DN3	B21	P3_TX_DP3
A22	GND	B22	GND
A23	P3_RX_DP2	B23	P3_TX_DN2
A24	P3_RX_DN2	B24	P3_TX_DP2
A25	GND	B25	GND
A26	SMB_MCIO3_SDA2	B26	MCIO3_2_BP_TYPE
A27	SMB_MCIO3_SCL2	B27	MCIO3_2_WAKE#
A28	GND	B28	GND
A29	MCIO3_USB2_P	B29	MCIO3_PERST_BUF2_N
A30	MCIO3_USB2_N	B30	MCIO3_CLKREQ
A31	GND	B31	GND
A32	P3_RX_DP1	B32	P3_TX_DN1
A33	P3_RX_DN1	B33	P3_TX_DP1
A34	GND	B34	GND
A35	P3_RX_DP0	B35	P3_TX_DN0
A36	P3_RX_DN0	B36	P3_TX_DP0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO4 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P3_RX_DP15	B2	P3_TX_DN15
A3	P3_RX_DN15	B3	P3_TX_DP15
A4	GND	B4	GND
A5	P3_RX_DP14	B5	P3_TX_DN14
A6	P3_RX_DN14	B6	P3_TX_DP14
A7	GND	B7	GND
A8	MCIO4_1_BP_TYPE	B8	SMB_MCIO4_SCL1
A9	MCIO4_1_WAKE#	B9	SMB_MCIO4_SDA1
A10	GND	B10	GND
A11	CLK_MCIO4_DP1	B11	MCIO4_PERST_BUF1_N
A12	CLK_MCIO4_DN1	B12	MCIO4_1_PRSNT_N
A13	GND	B13	GND
A14	P3_RX_DP13	B14	P3_TX_DN13
A15	P3_RX_DN13	B15	P3_TX_DP13
A16	GND	B16	GND
A17	P3_RX_DP12	B17	P3_TX_DN12
A18	P3_RX_DN12	B18	P3_TX_DP12
A19	GND	B19	GND
A20	P3_RX_DP11	B20	P3_TX_DN11
A21	P3_RX_DN11	B21	P3_TX_DP11
A22	GND	B22	GND
A23	P3_RX_DP10	B23	P3_TX_DN10
A24	P3_RX_DN10	B24	P3_TX_DP10
A25	GND	B25	GND
A26	SMB_MCIO4_SDA2	B26	MCIO4_2_BP_TYPE
A27	SMB_MCIO4_SCL2	B27	MCIO4_2_WAKE#
A28	GND	B28	GND
A29	MCIO4_USB2_P	B29	MCIO4_PERST_BUF2_N
A30	MCIO4_USB2_N	B30	MCIO4_CLKREQ
A31	GND	B31	GND
A32	P3_RX_DP9	B32	P3_TX_DN9
A33	P3_RX_DN9	B33	P3_TX_DP9
A34	GND	B34	GND
A35	P3_RX_DP8	B35	P3_TX_DN8
A36	P3_RX_DN8	B36	P3_TX_DP8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO5 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P1_RX_DN0	B2	P1_TX_DP0
A3	P1_RX_DP0	B3	P1_TX_DN0
A4	GND	B4	GND
A5	P1_RX_DN1	B5	P1_TX_DP1
A6	P1_RX_DP1	B6	P1_TX_DN1
A7	GND	B7	GND
A8	MCIO5_1_BP_TYPE	B8	SMB_MCIO5_SCL1
A9	MCIO5_1_WAKE#	B9	SMB_MCIO5_SDA1
A10	GND	B10	GND
A11	CLK_MCIO5_DP1	B11	MCIO5_PERST_BUF1_N
A12	CLK_MCIO5_DN1	B12	MCIO5_1_PRSNT_N
A13	GND	B13	GND
A14	P1_RX_DN2	B14	P1_TX_DP2
A15	P1_RX_DP2	B15	P1_TX_DN2
A16	GND	B16	GND
A17	P1_RX_DN3	B17	P1_TX_DP3
A18	P1_RX_DP3	B18	P1_TX_DN3
A19	GND	B19	GND
A20	P1_RX_DN4	B20	P1_TX_DP4
A21	P1_RX_DP4	B21	P1_TX_DN4
A22	GND	B22	GND
A23	P1_RX_DN5	B23	P1_TX_DP5
A24	P1_RX_DP5	B24	P1_TX_DN5
A25	GND	B25	GND
A26	SMB_MCIO5_SDA2	B26	MCIO5_2_BP_TYPE
A27	SMB_MCIO5_SCL2	B27	MCIO5_2_WAKE#
A28	GND	B28	GND
A29	MCIO5_USB2_P	B29	MCIO5_PERST_BUF2_N
A30	MCIO5_USB2_N	B30	MCIO5_CLKREQ
A31	GND	B31	GND
A32	P1_RX_DN6	B32	P1_TX_DP6
A33	P1_RX_DP6	B33	P1_TX_DN6
A34	GND	B34	GND
A35	P1_RX_DN7	B35	P1_TX_DP7
A36	P1_RX_DP7	B36	P1_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO6 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P1_RX_DN8	B2	P1_TX_DP8
A3	P1_RX_DP8	B3	P1_TX_DN8
A4	GND	B4	GND
A5	P1_RX_DN9	B5	P1_TX_DP9
A6	P1_RX_DP9	B6	P1_TX_DN9
A7	GND	B7	GND
A8	MCIO6_1_BP_TYPE	B8	SMB_MCIO6_SCL1
A9	MCIO6_1_WAKE#	B9	SMB_MCIO6_SDA1
A10	GND	B10	GND
A11	CLK_MCIO6_DP1	B11	MCIO6_PERST_BUF1_N
A12	CLK_MCIO6_DN1	B12	MCIO6_1_PRSNT_N
A13	GND	B13	GND
A14	P1_RX_DN10	B14	P1_TX_DP10
A15	P1_RX_DP10	B15	P1_TX_DN10
A16	GND	B16	GND
A17	P1_RX_DN11	B17	P1_TX_DP11
A18	P1_RX_DP11	B18	P1_TX_DN11
A19	GND	B19	GND
A20	P1_RX_DN12	B20	P1_TX_DP12
A21	P1_RX_DP12	B21	P1_TX_DN12
A22	GND	B22	GND
A23	P1_RX_DN13	B23	P1_TX_DP13
A24	P1_RX_DP13	B24	P1_TX_DN13
A25	GND	B25	GND
A26	SMB_MCIO6_SDA2	B26	MCIO6_2_BP_TYPE
A27	SMB_MCIO6_SCL2	B27	MCIO6_2_WAKE#
A28	GND	B28	GND
A29	MCIO6_USB2_P	B29	MCIO6_PERST_BUF2_N
A30	MCIO6_USB2_N	B30	MCIO6_CLKREQ
A31	GND	B31	GND
A32	P1_RX_DN14	B32	P1_TX_DP14
A33	P1_RX_DP14	B33	P1_TX_DN14
A34	GND	B34	GND
A35	P1_RX_DN15	B35	P1_TX_DP15
A36	P1_RX_DP15	B36	P1_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO7 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P0_RX_DN0	B2	P0_TX_DP0
A3	P0_RX_DP0	B3	P0_TX_DN0
A4	GND	B4	GND
A5	P0_RX_DN1	B5	P0_TX_DP1
A6	P0_RX_DP1	B6	P0_TX_DN1
A7	GND	B7	GND
A8	MCIO7_1_BP_TYPE	B8	SMB_MCIO7_SCL1
A9	MCIO7_1_WAKE#	B9	SMB_MCIO7_SDA1
A10	GND	B10	GND
A11	CLK_MCIO7_DP1	B11	MCIO7_PERST_BUF1_N
A12	CLK_MCIO7_DN1	B12	MCIO7_1_PRSNT_N
A13	GND	B13	GND
A14	P0_RX_DN2	B14	P0_TX_DP2
A15	P0_RX_DP2	B15	P0_TX_DN2
A16	GND	B16	GND
A17	P0_RX_DN3	B17	P0_TX_DP3
A18	P0_RX_DP3	B18	P0_TX_DN3
A19	GND	B19	GND
A20	P0_RX_DN4	B20	P0_TX_DP4
A21	P0_RX_DP4	B21	P0_TX_DN4
A22	GND	B22	GND
A23	P0_RX_DN5	B23	P0_TX_DP5
A24	P0_RX_DP5	B24	P0_TX_DN5
A25	GND	B25	GND
A26	SMB_MCIO7_SDA2	B26	MCIO7_2_BP_TYPE
A27	SMB_MCIO7_SCL2	B27	MCIO7_2_WAKE#
A28	GND	B28	GND
A29	MCIO7_USB2_P	B29	MCIO7_PERST_BUF2_N
A30	MCIO7_USB2_N	B30	MCIO7_CLKREQ
A31	GND	B31	GND
A32	P0_RX_DN6	B32	P0_TX_DP6
A33	P0_RX_DP6	B33	P0_TX_DN6
A34	GND	B34	GND
A35	P0_RX_DN7	B35	P0_TX_DP7
A36	P0_RX_DP7	B36	P0_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO8 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P0_RX_DN8	B2	P0_TX_DP8
A3	P0_RX_DP8	B3	P0_TX_DN8
A4	GND	B4	GND
A5	P0_RX_DN9	B5	P0_TX_DP9
A6	P0_RX_DP9	B6	P0_TX_DN9
A7	GND	B7	GND
A8	MCIO8_1_BP_TYPE	B8	SMB_MCIO8_SCL1
A9	MCIO8_1_WAKE#	B9	SMB_MCIO8_SDA1
A10	GND	B10	GND
A11	CLK_MCIO8_DP1	B11	MCIO8_PERST_BUF1_N
A12	CLK_MCIO8_DN1	B12	MCIO8_1_PRSNT_N
A13	GND	B13	GND
A14	P0_RX_DN10	B14	P0_TX_DP10
A15	P0_RX_DP10	B15	P0_TX_DN10
A16	GND	B16	GND
A17	P0_RX_DN11	B17	P0_TX_DP11
A18	P0_RX_DP11	B18	P0_TX_DN11
A19	GND	B19	GND
A20	P0_RX_DN12	B20	P0_TX_DP12
A21	P0_RX_DP12	B21	P0_TX_DN12
A22	GND	B22	GND
A23	P0_RX_DN13	B23	P0_TX_DP13
A24	P0_RX_DP13	B24	P0_TX_DN13
A25	GND	B25	GND
A26	SMB_MCIO8_SDA2	B26	MCIO8_2_BP_TYPE
A27	SMB_MCIO8_SCL2	B27	MCIO8_2_WAKE#
A28	GND	B28	GND
A29	MCIO8_USB2_P	B29	MCIO8_PERST_BUF2_N
A30	MCIO8_USB2_N	B30	MCIO8_CLKREQ
A31	GND	B31	GND
A32	P0_RX_DN14	B32	P0_TX_DP14
A33	P0_RX_DP14	B33	P0_TX_DN14
A34	GND	B34	GND
A35	P0_RX_DN15	B35	P0_TX_DP15
A36	P0_RX_DP15	B36	P0_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO9 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	G3_RX_DP0	B2	G3_TX_DP0
A3	G3_RX_DN0	B3	G3_TX_DN0
A4	GND	B4	GND
A5	G3_RX_DN1	B5	G3_TX_DP1
A6	G3_RX_DP1	B6	G3_TX_DN1
A7	GND	B7	GND
A8	MCIO9_1_BP_TYPE	B8	SMB_MCIO9_SCL1
A9	MCIO9_1_WKAE#	B9	SMB_MCIO9_SDA1
A10	GND	B10	GND
A11	CLK_MCIO9_DP1	B11	MCIO9_PERST_BUF1_N
A12	CLK_MCIO9_DN1	B12	MCIO9_1_PRSNT_N
A13	GND	B13	GND
A14	G3_RX_DN2	B14	G3_TX_DP2
A15	G3_RX_DP2	B15	G3_TX_DN2
A16	GND	B16	GND
A17	G3_RX_DN3	B17	G3_TX_DP3
A18	G3_RX_DP3	B18	G3_TX_DN3
A19	GND	B19	GND
A20	G3_RX_DN4	B20	G3_TX_DP4
A21	G3_RX_DP4	B21	G3_TX_DN4
A22	GND	B22	GND
A23	G3_RX_DN5	B23	G3_TX_DP5
A24	G3_RX_DP5	B24	G3_TX_DN5
A25	GND	B25	GND
A26	SMB_MCIO9_SDA2	B26	MCIO9_2_BP_TYPE
A27	SMB_MCIO9_SCL2	B27	MCIO9_2_WKAE#
A28	GND	B28	GND
A29	MCIO9_USB2_P	B29	MCIO9_PERST_BUF2_N
A30	MCIO9_USB2_N	B30	MCIO9_CLKREQ
A31	GND	B31	GND
A32	G3_RX_DN6	B32	G3_TX_DP6
A33	G3_RX_DP6	B33	G3_TX_DN6
A34	GND	B34	GND
A35	G3_RX_DN7	B35	G3_TX_DP7
A36	G3_RX_DP7	B36	G3_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO10 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	G3_RX_DN8	B2	G3_TX_DP8
A3	G3_RX_DP8	B3	G3_TX_DN8
A4	GND	B4	GND
A5	G3_RX_DN9	B5	G3_TX_DP9
A6	G3_RX_DP9	B6	G3_TX_DN9
A7	GND	B7	GND
A8	MCIO10_1_BP_TYPE	B8	SMB_MCIO10_SCL1
A9	MCIO10_1_WAKE#	B9	SMB_MCIO10_SDA1
A10	GND	B10	GND
A11	CLK_MCIO10_DP1	B11	MCIO10_PERST_BUF1_N
A12	CLK_MCIO10_DN1	B12	MCIO10_1_PRSNT_N
A13	GND	B13	GND
A14	G3_RX_DN10	B14	G3_TX_DP10
A15	G3_RX_DP10	B15	G3_TX_DN10
A16	GND	B16	GND
A17	G3_RX_DN11	B17	G3_TX_DP11
A18	G3_RX_DP11	B18	G3_TX_DN11
A19	GND	B19	GND
A20	G3_RX_DN12	B20	G3_TX_DP12
A21	G3_RX_DP12	B21	G3_TX_DN12
A22	GND	B22	GND
A23	G3_RX_DN13	B23	G3_TX_DP13
A24	G3_RX_DP13	B24	G3_TX_DN13
A25	GND	B25	GND
A26	SMB_MCIO10_SDA2	B26	MCIO10_2_BP_TYPE
A27	SMB_MCIO10_SCL2	B27	MCIO10_2_WKAE#
A28	GND	B28	GND
A29	MCIO10_USB2_P	B29	MCIO10_PERST_BUF2_N
A30	MCIO10_USB2_N	B30	MCIO10_CLKREQ
A31	GND	B31	GND
A32	G3_RX_DN14	B32	G3_TX_DP14
A33	G3_RX_DP14	B33	G3_TX_DN14
A34	GND	B34	GND
A35	G3_RX_DN15	B35	G3_TX_DP15
A36	G3_RX_DP15	B36	G3_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO11 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P2_RX_DP7	B2	P2_TX_DN7
A3	P2_RX_DN7	B3	P2_TX_DP7
A4	GND	B4	GND
A5	P2_RX_DP6	B5	P2_TX_DN6
A6	P2_RX_DN6	B6	P2_TX_DP6
A7	GND	B7	GND
A8	MCIO11_1_BP_TYPE	B8	SMB_MCIO11_SCL1
A9	MCIO11_1_WAKE#	B9	SMB_MCIO11_SDA1
A10	GND	B10	GND
A11	CLK_MCIO11_DP1	B11	MCIO11_PERST_BUF1_N
A12	CLK_MCIO11_DN1	B12	MCIO11_1_PRSNT_N
A13	GND	B13	GND
A14	P2_RX_DP5	B14	P2_TX_DN5
A15	P2_RX_DN5	B15	P2_TX_DP5
A16	GND	B16	GND
A17	P2_RX_DP4	B17	P2_TX_DN4
A18	P2_RX_DN4	B18	P2_TX_DP4
A19	GND	B19	GND
A20	P2_RX_DP3	B20	P2_TX_DN3
A21	P2_RX_DN3	B21	P2_TX_DP3
A22	GND	B22	GND
A23	P2_RX_DP2	B23	P2_TX_DN2
A24	P2_RX_DN2	B24	P2_TX_DP2
A25	GND	B25	GND
A26	SMB_MCIO11_SDA2	B26	MCIO11_2_BP_TYPE
A27	SMB_MCIO11_SCL2	B27	MCIO11_2_WAKE#
A28	GND	B28	GND
A29	MCIO11_USB2_P	B29	MCIO11_PERST_BUF2_N
A30	MCIO11_USB2_N	B30	MCIO11_CLKREQ
A31	GND	B31	GND
A32	P2_RX_DP1	B32	P2_TX_DN1
A33	P2_RX_DN1	B33	P2_TX_DP1
A34	GND	B34	GND
A35	P2_RX_DP0	B35	P2_TX_DN0
A36	P2_RX_DN0	B36	P2_TX_DP0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO12 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P2_RX_DP15	B2	P2_TX_DN15
A3	P2_RX_DN15	B3	P2_TX_DP15
A4	GND	B4	GND
A5	P2_RX_DP14	B5	P2_TX_DN14
A6	P2_RX_DN14	B6	P2_TX_DP14
A7	GND	B7	GND
A8	MCIO12_1_BP_TYPE	B8	SMB_MCIO12_SCL1
A9	MCIO12_1_WAKE#	B9	SMB_MCIO12_SDA1
A10	GND	B10	GND
A11	CLK_MCIO12_DP1	B11	MCIO12_PERST_BUF1_N
A12	CLK_MCIO12_DN1	B12	MCIO12_1_PRSNT_N
A13	GND	B13	GND
A14	P2_RX_DP13	B14	P2_TX_DN13
A15	P2_RX_DN13	B15	P2_TX_DP13
A16	GND	B16	GND
A17	P2_RX_DP12	B17	P2_TX_DN12
A18	P2_RX_DN12	B18	P2_TX_DP12
A19	GND	B19	GND
A20	P2_RX_DP11	B20	P2_TX_DN11
A21	P2_RX_DN11	B21	P2_TX_DP11
A22	GND	B22	GND
A23	P2_RX_DP10	B23	P2_TX_DN10
A24	P2_RX_DN10	B24	P2_TX_DP10
A25	GND	B25	GND
A26	SMB_MCIO12_SDA2	B26	MCIO12_2_BP_TYPE
A27	SMB_MCIO12_SCL2	B27	MCIO12_2_WAKE#
A28	GND	B28	GND
A29	MCIO12_USB2_P	B29	MCIO12_PERST_BUF2_N
A30	MCIO12_USB2_N	B30	MCIO12_CLKREQ
A31	GND	B31	GND
A32	P2_RX_DP9	B32	P2_TX_DN9
A33	P2_RX_DN9	B33	P2_TX_DP9
A34	GND	B34	GND
A35	P2_RX_DP8	B35	P2_TX_DN8
A36	P2_RX_DN8	B36	P2_TX_DP8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO13 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P3_RX_DN7	B2	P3_TX_DN7
A3	P3_RX_DP7	B3	P3_TX_DP7
A4	GND	B4	GND
A5	P3_RX_DP6	B5	P3_TX_DN6
A6	P3_RX_DN6	B6	P3_TX_DP6
A7	GND	B7	GND
A8	MCIO13_1_BP_TYPE	B8	SMB_MCIO13_SCL1
A9	MCIO13_1_WAKE#	B9	SMB_MCIO13_SDA1
A10	GND	B10	GND
A11	CLK_MCIO13_DP1	B11	MCIO13_PERST_BUF1_N
A12	CLK_MCIO13_DN1	B12	MCIO13_1_PRSNT_N
A13	GND	B13	GND
A14	P3_RX_DP5	B14	P3_TX_DN5
A15	P3_RX_DN5	B15	P3_TX_DP5
A16	GND	B16	GND
A17	PE0_RX_DP4	B17	P3_TX_DN4
A18	PE0_RX_DN4	B18	P3_TX_DP4
A19	GND	B19	GND
A20	P3_RX_DP3	B20	P3_TX_DN3
A21	P3_RX_DN3	B21	P3_TX_DP3
A22	GND	B22	GND
A23	P3_RX_DP2	B23	P3_TX_DN2
A24	P3_RX_DN2	B24	P3_TX_DP2
A25	GND	B25	GND
A26	SMB_MCIO13_SDA2	B26	MCIO13_2_BP_TYPE
A27	SMB_MCIO13_SCL2	B27	MCIO13_2_WAKE#
A28	GND	B28	GND
A29	MCIO13_USB2_P	B29	MCIO13_PERST_BUF2_N
A30	MCIO13_USB2_N	B30	MCIO13_CLKREQ
A31	GND	B31	GND
A32	P3_RX_DP1	B32	P3_TX_DN1
A33	P3_RX_DN1	B33	P3_TX_DP1
A34	GND	B34	GND
A35	P3_RX_DP0	B35	P3_TX_DN0
A36	P3_RX_DN0	B36	P3_TX_DP0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO14 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P3_RX_DP15	B2	P3_TX_DN15
A3	P3_RX_DN15	B3	P3_TX_DP15
A4	GND	B4	GND
A5	P3_RX_DP14	B5	P3_TX_DN14
A6	P3_RX_DN14	B6	P3_TX_DP14
A7	GND	B7	GND
A8	MCIO14_1_BP_TYPE	B8	SMB_MCIO14_SCL1
A9	MCIO14_1_WAKE#	B9	SMB_MCIO14_SDA1
A10	GND	B10	GND
A11	CLK_MCIO14_DP1	B11	MCIO14_PERST_BUF1_N
A12	CLK_MCIO14_DN1	B12	MCIO14_1_PRSNT_N
A13	GND	B13	GND
A14	P3_RX_DP13	B14	P3_TX_DN13
A15	P3_RX_DN13	B15	P3_TX_DP13
A16	GND	B16	GND
A17	P3_RX_DP12	B17	P3_TX_DN12
A18	P3_RX_DN12	B18	P3_TX_DP12
A19	GND	B19	GND
A20	P3_RX_DP11	B20	P3_TX_DN11
A21	P3_RX_DN11	B21	P3_TX_DP11
A22	GND	B22	GND
A23	P3_RX_DP10	B23	P3_TX_DN10
A24	P3_RX_DN10	B24	P3_TX_DP10
A25	GND	B25	GND
A26	SMB_MCIO14_SDA2	B26	MCIO14_2_BP_TYPE
A27	SMB_MCIO14_SCL2	B27	MCIO14_2_WAKE#
A28	GND	B28	GND
A29	MCIO14_USB2_P	B29	MCIO14_PERST_BUF2_N
A30	MCIO14_USB2_N	B30	MCIO14_CLKREQ
A31	GND	B31	GND
A32	P3_RX_DP9	B32	P3_TX_DN9
A33	P3_RX_DN9	B33	P3_TX_DP9
A34	GND	B34	GND
A35	P3_RX_DP8	B35	P3_TX_DN8
A36	P3_RX_DN8	B36	P3_TX_DP8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO15 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P1_RX_DN0	B2	P1_TX_DP0
A3	P1_RX_DP0	B3	P1_TX_DN0
A4	GND	B4	GND
A5	P1_RX_DN1	B5	P1_TX_DP1
A6	P1_RX_DP1	B6	P1_TX_DN1
A7	GND	B7	GND
A8	MCIO15_1_BP_TYPE	B8	SMB_MCIO15_SCL1
A9	MCIO15_1_WAKE#	B9	SMB_MCIO15_SDA1
A10	GND	B10	GND
A11	CLK_MCIO15_DP1	B11	MCIO15_PERST_BUF1_N
A12	CLK_MCIO15_DN1	B12	MCIO15_1_PRSNT_N
A13	GND	B13	GND
A14	P1_RX_DN2	B14	P1_TX_DP2
A15	P1_RX_DP2	B15	P1_TX_DN2
A16	GND	B16	GND
A17	P1_RX_DN3	B17	P1_TX_DP3
A18	P1_RX_DP3	B18	P1_TX_DN3
A19	GND	B19	GND
A20	P1_RX_DN4	B20	P1_TX_DP4
A21	P1_RX_DP4	B21	P1_TX_DN4
A22	GND	B22	GND
A23	P1_RX_DN5	B23	P1_TX_DP5
A24	P1_RX_DP5	B24	P1_TX_DN5
A25	GND	B25	GND
A26	SMB_MCIO15_SDA2	B26	MCIO15_2_BP_TYPE
A27	SMB_MCIO15_SCL2	B27	MCIO15_2_WAKE#
A28	GND	B28	GND
A29	MCIO15_USB2_P	B29	MCIO15_PERST_BUF2_N
A30	MCIO15_USB2_N	B30	MCIO15_CLKREQ
A31	GND	B31	GND
A32	P1_RX_DN6	B32	P1_TX_DP6
A33	P1_RX_DP6	B33	P1_TX_DN6
A34	GND	B34	GND
A35	P1_RX_DN7	B35	P1_TX_DP7
A36	P1_RX_DP7	B36	P1_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO16 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P1_RX_DN8	B2	P1_TX_DP8
A3	P1_RX_DP8	B3	P1_TX_DN8
A4	GND	B4	GND
A5	P1_RX_DN9	B5	P1_TX_DP9
A6	P1_RX_DP9	B6	P1_TX_DN9
A7	GND	B7	GND
A8	MCIO16_1_BP_TYPE	B8	SMB_MCIO16_SCL1
A9	MCIO16_1_WAKE#	B9	SMB_MCIO16_SDA1
A10	GND	B10	GND
A11	CLK_MCIO16_DP1	B11	MCIO16_PERST_BUF1_N
A12	CLK_MCIO16_DN1	B12	MCIO16_1_PRSNT_N
A13	GND	B13	GND
A14	P1_RX_DN10	B14	P1_TX_DP10
A15	P1_RX_DP10	B15	P1_TX_DN10
A16	GND	B16	GND
A17	P1_RX_DN11	B17	P1_TX_DP11
A18	P1_RX_DP11	B18	P1_TX_DN11
A19	GND	B19	GND
A20	P1_RX_DN12	B20	P1_TX_DP12
A21	P1_RX_DP12	B21	P1_TX_DN12
A22	GND	B22	GND
A23	P1_RX_DN13	B23	P1_TX_DP13
A24	P1_RX_DP13	B24	P1_TX_DN13
A25	GND	B25	GND
A26	SMB_MCIO16_SDA2	B26	MCIO16_2_BP_TYPE
A27	SMB_MCIO16_SCL2	B27	MCIO16_2_WAKE#
A28	GND	B28	GND
A29	MCIO16_USB2_P	B29	MCIO16_PERST_BUF2_N
A30	MCIO16_USB2_N	B30	MCIO16_CLKREQ
A31	GND	B31	GND
A32	P1_RX_DN14	B32	P1_TX_DP14
A33	P1_RX_DP14	B33	P1_TX_DN14
A34	GND	B34	GND
A35	P1_RX_DN15	B35	P1_TX_DP15
A36	P1_RX_DP15	B36	P1_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO17 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P0_RX_DN0	B2	P0_TX_DP0
A3	P0_RX_DP0	B3	P0_TX_DN0
A4	GND	B4	GND
A5	P0_RX_DN1	B5	P0_TX_DP1
A6	P0_RX_DP1	B6	P0_TX_DN1
A7	GND	B7	GND
A8	MCIO17_1_BP_TYPE	B8	SMB_MCIO17_SCL1
A9	MCIO17_1_WAKE#	B9	SMB_MCIO17_SDA1
A10	GND	B10	GND
A11	CLK_MCIO17_DP1	B11	MCIO17_PERST_BUF1_N
A12	CLK_MCIO17_DN1	B12	MCIO17_1_PRSNT_N
A13	GND	B13	GND
A14	P0_RX_DN2	B14	P0_TX_DP2
A15	P0_RX_DP2	B15	P0_TX_DN2
A16	GND	B16	GND
A17	P0_RX_DN3	B17	P0_TX_DP3
A18	P0_RX_DP3	B18	P0_TX_DN3
A19	GND	B19	GND
A20	P0_RX_DN4	B20	P0_TX_DP4
A21	P0_RX_DP4	B21	P0_TX_DN4
A22	GND	B22	GND
A23	P0_RX_DN5	B23	P0_TX_DP5
A24	P0_RX_DP5	B24	P0_TX_DN5
A25	GND	B25	GND
A26	SMB_MCIO17_SDA2	B26	MCIO17_2_BP_TYPE
A27	SMB_MCIO17_SCL2	B27	MCIO17_2_WAKE#
A28	GND	B28	GND
A29	MCIO17_USB2_P	B29	MCIO17_PERST_BUF2_N
A30	MCIO17_USB2_N	B30	MCIO17_CLKREQ
A31	GND	B31	GND
A32	P0_RX_DN6	B32	P0_TX_DP6
A33	P0_RX_DP6	B33	P0_TX_DN6
A34	GND	B34	GND
A35	P0_RX_DN7	B35	P0_TX_DP7
A36	P0_RX_DP7	B36	P0_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO18 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	P0_RX_DN8	B2	P0_TX_DP8
A3	P0_RX_DP8	B3	P0_TX_DN8
A4	GND	B4	GND
A5	P0_RX_DN9	B5	P0_TX_DP9
A6	P0_RX_DP9	B6	P0_TX_DN9
A7	GND	B7	GND
A8	MCIO18_1_BP_TYPE	B8	SMB_MCIO18_SCL1
A9	MCIO18_1_WAKE#	B9	SMB_MCIO18_SDA1
A10	GND	B10	GND
A11	CLK_MCIO18_DP1	B11	MCIO18_PERST_BUF1_N
A12	CLK_MCIO18_DN1	B12	MCIO18_1_PRSNT_N
A13	GND	B13	GND
A14	P0_RX_DN10	B14	P0_TX_DP10
A15	P0_RX_DP10	B15	P0_TX_DN10
A16	GND	B16	GND
A17	P0_RX_DN11	B17	P0_TX_DP11
A18	P0_RX_DP11	B18	P0_TX_DN11
A19	GND	B19	GND
A20	P0_RX_DN12	B20	P0_TX_DP12
A21	P0_RX_DP12	B21	P0_TX_DN12
A22	GND	B22	GND
A23	P0_RX_DN13	B23	P0_TX_DP13
A24	P0_RX_DP13	B24	P0_TX_DN13
A25	GND	B25	GND
A26	SMB_MCIO18_SDA2	B26	MCIO18_2_BP_TYPE
A27	SMB_MCIO18_SCL2	B27	MCIO18_2_WAKE#
A28	GND	B28	GND
A29	MCIO18_USB2_P	B29	MCIO18_PERST_BUF2_N
A30	MCIO18_USB2_N	B30	MCIO18_CLKREQ
A31	GND	B31	GND
A32	P0_RX_DN14	B32	P0_TX_DP14
A33	P0_RX_DP14	B33	P0_TX_DN14
A34	GND	B34	GND
A35	P0_RX_DN15	B35	P0_TX_DP15
A36	P0_RX_DP15	B36	P0_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO19 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	G1_RX_DN0	B2	G1_TX_DP0
A3	G1_RX_DP0	B3	G1_TX_DN0
A4	GND	B4	GND
A5	G1_RX_DN1	B5	G1_TX_DP1
A6	G1_RX_DP1	B6	G1_TX_DN1
A7	GND	B7	GND
A8	MCIO19_1_BP_TYPE	B8	SMB_MCIO19_SCL1
A9	MCIO19_1_WAKE#	B9	SMB_MCIO19_SDA1
A10	GND	B10	GND
A11	CLK_MCIO19_DP1	B11	MCIO19_PERST_BUF1_N
A12	CLK_MCIO19_DN1	B12	MCIO19_1_PRSNT_N
A13	GND	B13	GND
A14	G1_RX_DN2	B14	G1_TX_DP2
A15	G1_RX_DP2	B15	G1_TX_DN2
A16	GND	B16	GND
A17	G1_RX_DN3	B17	G1_TX_DP3
A18	G1_RX_DP3	B18	G1_TX_DN3
A19	GND	B19	GND
A20	G1_RX_DN4	B20	G1_TX_DP4
A21	G1_RX_DP4	B21	G1_TX_DN4
A22	GND	B22	GND
A23	G1_RX_DN5	B23	G1_TX_DP5
A24	G1_RX_DP5	B24	G1_TX_DN5
A25	GND	B25	GND
A26	SMB_MCIO19_SDA2	B26	MCIO19_2_BP_TYPE
A27	SMB_MCIO19_SCL2	B27	MCIO19_2_WAKE#
A28	GND	B28	GND
A29	MCIO19_USB2_P	B29	MCIO19_PERST_BUF2_N
A30	MCIO19_USB2_N	B30	MCIO19_CLKREQ
A31	GND	B31	GND
A32	G1_RX_DN6	B32	G1_TX_DP6
A33	G1_RX_DP6	B33	G1_TX_DN6
A34	GND	B34	GND
A35	G1_RX_DN7	B35	G1_TX_DP7
A36	G1_RX_DP7	B36	G1_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO20 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	G1_RX_DN8	B2	G1_TX_DP8
A3	G1_RX_DP8	B3	G1_TX_DN8
A4	GND	B4	GND
A5	G1_RX_DN9	B5	G1_TX_DP9
A6	G1_RX_DP9	B6	G1_TX_DN9
A7	GND	B7	GND
A8	MCIO20_1_BP_TYPE	B8	SMB_MCIO20_SCL1
A9	MCIO20_1_WAKE#	B9	SMB_MCIO20_SDA1
A10	GND	B10	GND
A11	CLK_MCIO20_DP1	B11	MCIO20_PERST_BUF1_N
A12	CLK_MCIO20_DN1	B12	MCIO20_1_PRSNT_N
A13	GND	B13	GND
A14	G1_RX_DN10	B14	G1_TX_DP10
A15	G1_RX_DP10	B15	G1_TX_DN10
A16	GND	B16	GND
A17	G1_RX_DN11	B17	G1_TX_DP11
A18	G1_RX_DP11	B18	G1_TX_DN11
A19	GND	B19	GND
A20	G1_RX_DN12	B20	G1_TX_DP12
A21	G1_RX_DP12	B21	G1_TX_DN12
A22	GND	B22	GND
A23	G1_RX_DN13	B23	G1_TX_DP13
A24	G1_RX_DP13	B24	G1_TX_DN13
A25	GND	B25	GND
A26	SMB_MCIO20_SDA2	B26	MCIO20_2_BP_TYPE
A27	SMB_MCIO20_SCL2	B27	MCIO20_2_WAKE#
A28	GND	B28	GND
A29	MCIO20_USB2_P	B29	MCIO20_PERST_BUF2_N
A30	MCIO20_USB2_N	B30	MCIO20_CLKREQ
A31	GND	B31	GND
A32	G1_RX_DN14	B32	G1_TX_DP14
A33	G1_RX_DP14	B33	G1_TX_DN14
A34	GND	B34	GND
A35	G1_RX_DP15	B35	G1_TX_DP15
A36	G1_RX_DN15	B36	G1_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

2.8 Dr. Debug

Dr. Debug is used to provide code information, which makes troubleshooting even easier. Please see the diagrams below for reading the Dr. Debug codes.

Code	Description
0x10	PEI_CORE_STARTED
0x11	PEI_CAR_CPU_INIT
0x15	PEI_CAR_NB_INIT
0x19	PEI_CAR_SB_INIT
0x31	PEI_MEMORY_INSTALLED
0x32	PEI_CPU_INIT
0x33	PEI_CPU_CACHE_INIT
0x34	PEI_CPU_AP_INIT
0x35	PEI_CPU_BSP_SELECT
0x36	PEI_CPU_SMM_INIT
0x37	PEI_MEM_NB_INIT
0x3B	PEI_MEM_SB_INIT
0x4F	PEI_DXE_IPL_STARTED
0x60	DXE_CORE_STARTED
0x61	DXE_NVRAM_INIT
0x62	DXE_SBRUN_INIT

0x63	DXE_CPU_INIT
0x68	DXE_NB_HB_INIT
0x69	DXE_NB_INIT
0x6A	DXE_NB_SMM_INIT
0x70	DXE_SB_INIT
0x71	DXE_SB_SMM_INIT
0x72	DXE_SB_DEVICES_INIT
0x78	DXE_ACPI_INIT
0x79	DXE_CSM_INIT
0x90	DXE_BDS_STARTED
0x91	DXE_BDS_CONNECT_DRIVERS
0x92	DXE_PCI_BUS_BEGIN
0x93	DXE_PCI_BUS_HPC_INIT
0x94	DXE_PCI_BUS_ENUM
0x95	DXE_PCI_BUS_REQUEST_RESOURCES
0x96	DXE_PCI_BUS_ASSIGN_RESOURCES
0x97	DXE_CON_OUT_CONNECT
0x98	DXE_CON_IN_CONNECT

0x99	DXE_SIO_INIT
0x9A	DXE_USB_BEGIN
0x9B	DXE_USB_RESET
0x9C	DXE_USB_DETECT
0x9D	DXE_USB_ENABLE
0xA0	DXE_IDE_BEGIN
0xA1	DXE_IDE_RESET
0xA2	DXE_IDE_DETECT
0xA3	DXE_IDE_ENABLE
0xA4	DXE_SCSI_BEGIN
0xA5	DXE_SCSI_RESET
0xA6	DXE_SCSI_DETECT
0xA7	DXE_SCSI_ENABLE
0xA8	DXE_SETUP_VERIFYING_PASSWORD
0xA9	DXE_SETUP_START
0xAB	DXE_SETUP_INPUT_WAIT
0xAD	DXE_READY_TO_BOOT
0xAE	DXE_LEGACY_BOOT

0xAF	DXE_EXIT_BOOT_SERVICES
0xB0	RT_SET_VIRTUAL_ADDRESS_MAP_BEGIN
0xB1	RT_SET_VIRTUAL_ADDRESS_MAP_END
0xB2	DXE_LEGACY_OPROM_INIT
0xB3	DXE_RESET_SYSTEM
0xB4	DXE_USB_HOTPLUG
0xB5	DXE_PCI_BUS_HOTPLUG
0xB6	DXE_NVRAM_CLEANUP
0xB7	DXE_CONFIGURATION_RESET
0xF0	PEI_RECOVERY_AUTO
0xF1	PEI_RECOVERY_USER
0xF2	PEI_RECOVERY_STARTED
0xF3	PEI_RECOVERY_CAPSULE_FOUND
0xF4	PEI_RECOVERY_CAPSULE_LOADED
0xE0	PEI_S3_STARTED
0xE1	PEI_S3_BOOT_SCRIPT
0xE2	PEI_S3_VIDEO_REPOST

0xE3	PEI_S3_OS_WAKE
0x50	PEI_MEMORY_INVALID_TYPE
0x53	PEI_MEMORY_NOT_DETECTED
0x55	PEI_MEMORY_NOT_INSTALLED
0x57	PEI_CPU_MISMATCH
0x58	PEI_CPU_SELF_TEST_FAILED
0x59	PEI_CPU_NO_MICROCODE
0x5A	PEI_CPU_ERROR
0x5B	PEI_RESET_NOT_AVAILABLE
0xD0	DXE_CPU_ERROR
0xD1	DXE_NB_ERROR
0xD2	DXE_SB_ERROR
0xD3	DXE_ARCH_PROTOCOL_NOT_AVAILABLE
0xD4	DXE_PCI_BUS_OUT_OF_RESOURCES
0xD5	DXE_LEGACY_OPROM_NO_SPACE
0xD6	DXE_NO_CON_OUT
0xD7	DXE_NO_CON_IN

0xD8	DXE_INVALID_PASSWORD
0xD9	DXE_BOOT_OPTION_LOAD_ERROR
0xDA	DXE_BOOT_OPTION_FAILED
0xDB	DXE_FLASH_UPDATE_FAILED
0xDC	DXE_RESET_NOT_AVAILABLE
0xE8	PEI_MEMORY_S3_RESUME_FAILED
0xE9	PEI_S3_RESUME_PPI_NOT_FOUND
0xEA	PEI_S3_BOOT_SCRIPT_ERROR
0xEB	PEI_S3_OS_WAKE_ERROR

2.9 Dual LAN and Teaming Operation Guide

Dual LAN with Teaming enabled on this motherboard allows two single connections to act as one single connection(s) for twice the transmission bandwidth, making data transmission more effective and improving the quality of transmission of distant images. Fault tolerance on the dual LAN network prevents network downtime by transferring the workload from a failed port to a working port.

The speed of transmission is subject to the actual network environment or status even with Teaming enabled.

Before setting up Teaming, please make sure whether the Switch (or Router) supports Teaming (IEEE 802.3ad Link Aggregation). Specify a preferred adapter in Intel PROSet. Under normal conditions, the Primary adapter handles all non-TCP/IP traffic. The Secondary adapter will receive fallback traffic if the primary fails. If the Preferred Primary adapter fails, but is later restored to an active status, control is automatically switched back to the Preferred Primary adapter.

Step 1

From **Device Manager**, open the properties of a team.

Step 2

Click the **Settings** tab.

Step 3

Click the **Modify Team** button.

Step 4

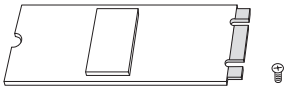
Select the adapter to the primary adapter and click the **Set Primary** button.

If it does not specify a preferred primary adapter, the software will choose an adapter of the highest capability (model and speed) to act as the default primary. If a failover occurs, another adapter becomes the primary. The adapter will, however, rejoin the team as a non-primary.

2.10 M.2_SSD Module Installation Guide

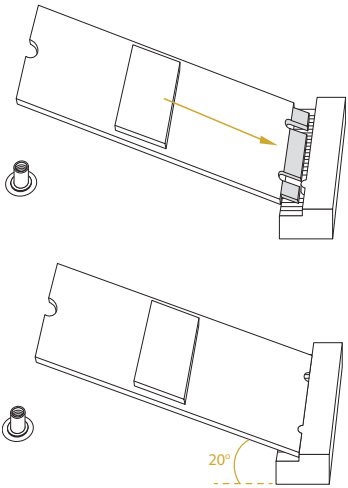
The M.2 Socket (M2_1/M2_2, Key M) supports type 2280 M.2 PCI Express module and up to Gen5 x4.

Installing the M.2_SSD Module



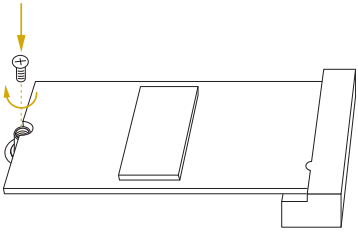
Step 1

Prepare a M.2 SSD module and the screw.



Step 2

Align and gently insert the M.2 SSD module into the M.2 slot. Please be aware that the M.2 SSD module only fits in one orientation.



Step 3

Tighten the screw with a screwdriver to secure the module into place. Please do not overtighten the screw as this might damage the module.

Chapter 3 UEFI Setup Utility

3.1 Introduction

This section explains how to use the UEFI SETUP UTILITY to configure the system. The UEFI chip on the motherboard stores the UEFI SETUP UTILITY. Run the UEFI SETUP UTILITY when starting up the computer. Please press <F2> or <Del> during the Power-On-Self-Test (POST) to enter the UEFI SETUP UTILITY; otherwise, POST will continue with its test routines.

Restart the system by pressing <Ctrl> + <Alt> + <Delete> to enter the UEFI SETUP UTI ITY after POST, or by pressing the reset button on the system chassis. This allows user to restart by turning the system off and then back on.

Because the UEFI software is constantly being updated, the following UEFI setup screens and descriptions are for reference purpose only, and they may not exactly match what seeing on the screen.

3.1.1 UEFI Menu Bar

The top of the screen has a menu bar with the following selections:

Item	Description
Main	To set up the system time/date information
Advanced	To set up the advanced UEFI features
Server Mgmt	To manage the server
Event Logs	For event log configuration
Security	To set up the security features
Boot	To set up the default system device to locate and load the Operating System
Exit	To exit the current screen or the UEFI SETUP UTILITY

Use < ← > key or < → > key to choose among the selections on the menu bar, and then press <Enter> to get into the sub screen.

English

3.1.2 Navigation Keys

Please check the following table for the function description of each navigation key.

Navigation Key(s)	Function Description
← / →	Moves cursor left or right to select Screens
↑ / ↓	Moves cursor up or down to select items
+ / -	To change option for the selected items
<Tab>	Switch to next function
<Enter>	To bring up the selected screen
<PGUP>	Go to the previous page
<PGDN>	Go to the next page
<HOME>	Go to the top of the screen
<END>	Go to the bottom of the screen
<F1>	To display the General Help Screen
<F7>	Discard changes and exit the UEFI SETUP UTILITY
<F9>	Load optimal default values for all the settings
<F10>	Save changes and exit the UEFI SETUP UTILITY
<F12>	Print screen
<ESC>	Jump to the Exit Screen or exit the current screen

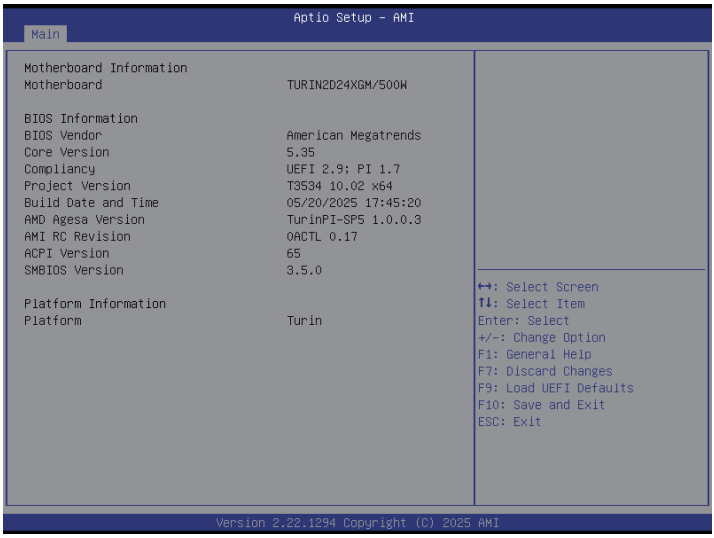
3.2 Main Screen

Once entering the UEFI SETUP UTILITY, the Main screen will appear and display the system overview. The Main screen provides system overview information and allows user-to set the system time and date.

The screenshots in this user manual are examples and for references only. The actual images may slightly vary depending on the model and the version used.

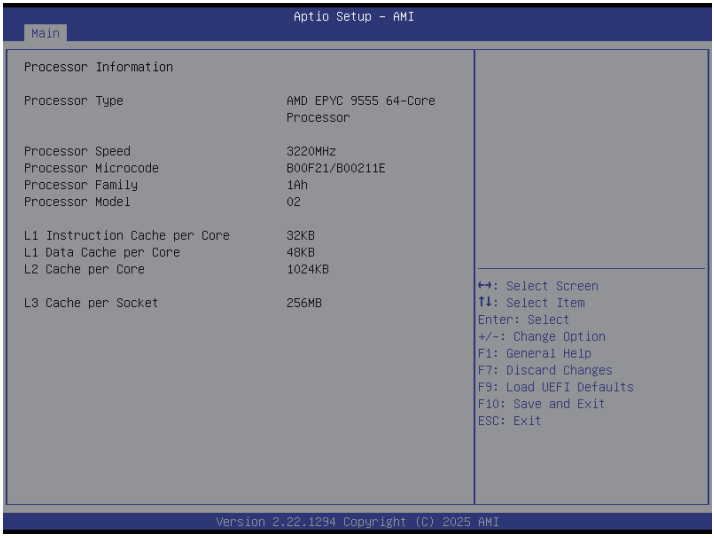
3.2.1 Mother Board Information

Press <Enter> to view the information of the motheboard.



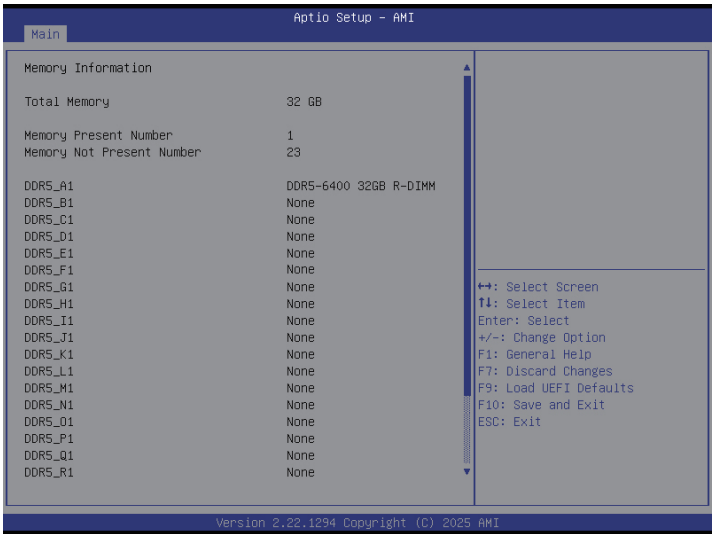
3.2.2 Processor Information

Press <Enter> to view the information of the processor.



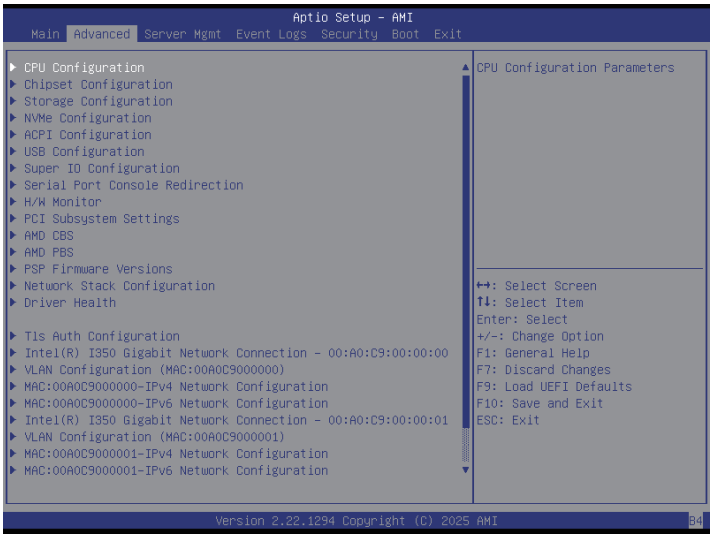
3.2.3 Memory Information

Press <Enter> to view the information of the memory.



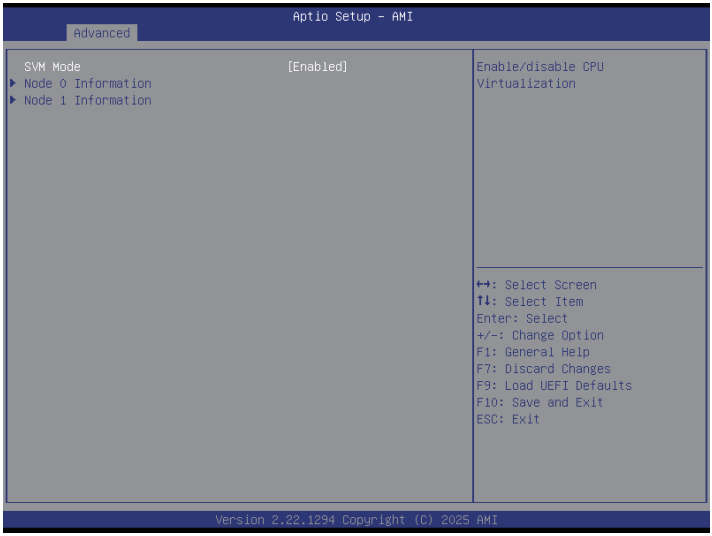
3.3 Advanced Screen

In this section, set the configurations for the following items: CPU Configuration, Chipset Configuration, Storage Configuration, NVMe Configuration, ACPI Configuration, USB Configuration, Super IO Configuration, Serial Port Console Redirection, H/W Monitor, PCI Subsystem Settings, AMD CBS, AMD PBS, PSP Firmware Versions, Network Stack-Configuration, Driver Health, Tls Auth Configuration and Instant Flash.



Setting wrong values in this section may cause the system to malfunction.

3.3.1 CPU Configuration



SVM Mode

Enable/disable CPU Virtualization.

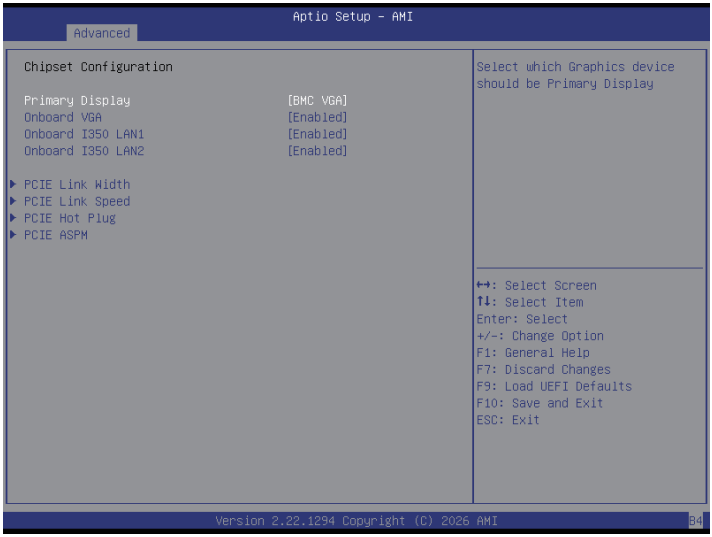
Node 0 Information

Use this item to view Information related to Node 0.

Node 1 Information

Use this item to view Information related to Node 1.

3.3.2 Chipset Configuration



Primary Display

Select which Graphics device should be Primary Display.

Onboard VGA

Use this item to enable or disable the onboard VGA function.

Onboard I350 LAN1

Use this item to enable or disable the onboard LAN1 function.

Onboard I350 LAN2

Use this item to enable or disable the onboard LAN2 function.

PCIE Link Width

Select this item to configure PCIE Link Width.

MCIO2/MCIO1, MCIO4/MCIO3, MCIO6/MCIO5, MCIO8/MCIO7, MCIO10/MCIO9, MCIO12/MCIO11, MCIO14/MCIO13, MCIO16/MCIO15, MCIO18/MCIO17, MCIO20/MCIO19 Link Width

Select PCIe port Bifurcation for MCIO, the default value is [x4x4/x4x4]. Options: [x16], [x8x8], [x8/x4x4], [x4x4/x8] and [x4x4/x4x4].

PCIE Link Speed

Select PCIE Link Speed.

MCIO9/MCIO10/MCIO19/MCIO20 Link Speed
Select PCIE Link Speed, [Auto] means up to Gen5 (32GT/s).

PCIE Hot Plug

Select this item to configure PCIE Hot Plug globally.

MCIO1/MCIO2/MCIO3/MCIO4/MCIO5/MCIO6/ MCIO7/MCIO8/MCIO9/ MCIO10/MCIO11/MCIO12/MCIO13/MCIO14/MCIO15/MCIO16/MCIO17/ MCIO18/MCIO19/MCIO20 Hot Plug
Enable or disable PCIE Hot Plug.

PCIE ASPM

Selec this item to configure the PCIE ASPM.

PCI-E ASPM Support (Global)
Select this item to disable ASPM Support in all PCIe root ports.

MCIO1/MCIO2/MCIO3/MCIO4/MCIO5/MCIO6/ MCIO7/MCIO8/MCIO9/ MCIO10/MCIO11/MCIO12/MCIO13/MCIO14/MCIO15/MCIO16/MCIO17/ MCIO18/MCIO19/MCIO20 ASPM Support
Select this item to configure PCI Express Active State Power Management settings.

3.3.3 Storage Configuration

Hard Disk S.M.A.R.T.

S.M.A.R.T stands for Self-Monitoring, Analysis, and Reporting Technology. It is a monitoring system for computer hard disk drives to detect and report on various indicators of reliability.

SATA Hot Plug

Designates All SATA port as Hot Pluggable.

3.3.4 NVMe Configuration

The NVMe Configuration displays the NVMe Drive Options Settings.

Launch NVMe driver

Select this item to enable or disable launch NVMe driver.

3.3.5 ACPI Configuration

PCIE Devices Power On

Allow the system to be waked up by a PCIE device and enable wake on LAN.

Ring-In Power On

Allow the system to be waked up by onboard COM port modem Ring-In Singals.

RTC Alarm Power On

Allow the system to be waked up by real time clock alarm. Set it to By OS to let it be handled by the operating system.

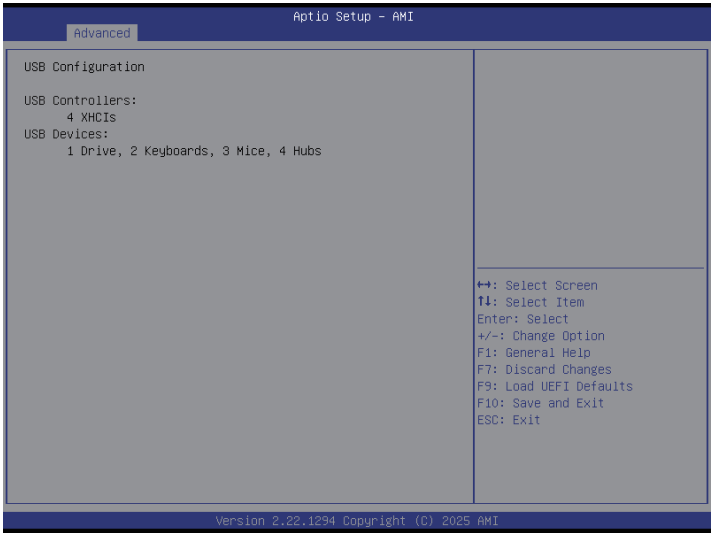
RTC Alarm Date
Use this item to set Date of RTC power on feature.

RTC Alarm Hour
Use this item to set Hour of RTC power on feature.

RTC Alarm Minute
Use this item to set Minute of RTC power on feature.

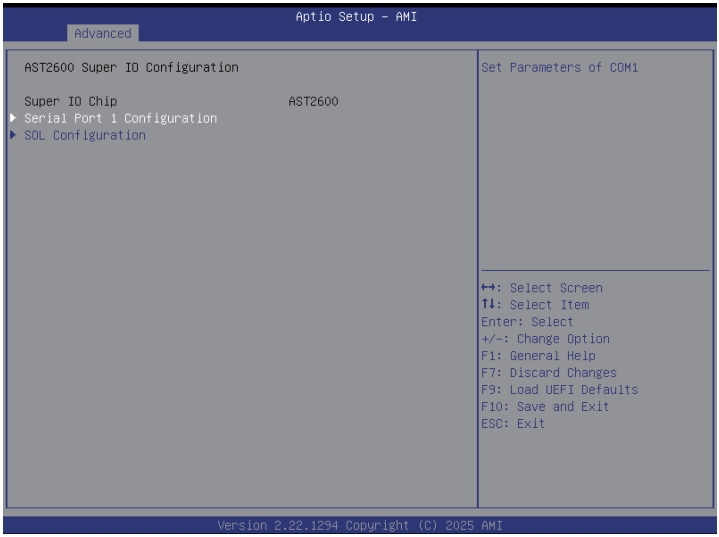
RTC Alarm Second
Use this item to set Second of RTC power on feature.

3.3.6 USB Configuration



This displays the USB Controllers and USB Devices information.

3.3.7 Super IO Configuration



Serial Port 1 Configuration

Use this item to set parameters of Serial Port 1 (COMA).

Serial Port

Use this item to enable or disable the Serial Port (COM).

Change Settings

Use this item to select an optimal setting for Super IO device.

SOL Configuration

Use this item to set parameters of Serial Port 2 (COMB).

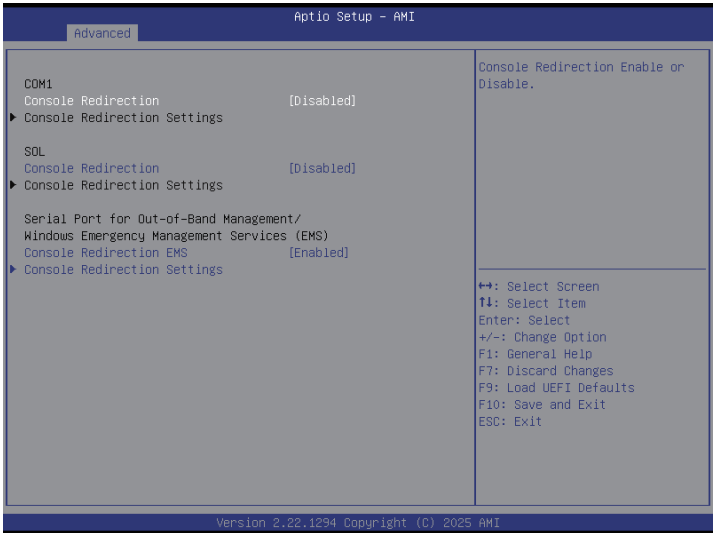
SOL Port

Use this item to enable or disable the Serial Port (COM).

Change Settings

Use this item to select an optimal setting for Super IO device.

3.3.8 Serial Port Console Redirection



COM1 / SOL

Console Redirection

Use this option to enable or disable Console Redirection. If this item is set to Enabled, user can select a COM Port to be used for Console Redirection.

Console Redirection Settings

Use this option to configure Console Redirection Settings, and specify how the computer and the host computer to which are connected exchange information. Both computers should have the same or compatible settings.

Terminal Type

Use this item to select the preferred terminal emulation type for out-of-band management. It is recommended to select [VT-UTF8].

Option	Description
VT100	ASCII character set
VT100Plus	Extended VT100 that supports color and function keys
VT-UTF8	UTF8 encoding is used to map Unicode chars onto 1 or more bytes
ANSI	Extended ASCII character set

Bits Per Second
Use this item to select the serial port transmission speed. The speed used in the host computer and the client computer must be the same. Long or noisy lines may require lower transmission speed. The options include [9600], [19200], [38400], [57600] and [115200].

Data Bits
Use this item to set the data transmission size. The options include [7] and [8] (Bits).

Parity
Use this item to select the parity bit. The options include [None], [Even], [Odd], [Mark] and [Space].

Stop Bits
The item indicates the end of a serial data packet. The standard setting is [1] Stop Bit. Select [2] Stop Bits for slower devices.

Flow Control
Use this item to set the flow control to prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a "stop" signal can be sent to stop the data flow. Once the buffers are empty, a "start" signal can be sent to restart the flow. Hardware flow uses two wires to send start/stop signals. The options include [None] and [Hardware RTS/CTS].

VT-UTF8 Combo Key Support
Use this item to enable or disable the VT-UTF8 Combo Key Support for ANSI/VT100 terminals.

Recorder Mode
Use this item to enable or disable Recorder Mode to capture terminal data and send it as text messages.

Resolution 100x31
Use this item to enable or disable extended terminal resolution support.

Putty Keypad
Use this item to select Function Key and Keypad on Putty.

Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS)

Console Redirection EMS

Use this option to enable or disable Console Redirection EMS. If this item is set to Enabled, user can select a COM Port to be used for Console Redirection.

Console Redirection Settings

Use this option to configure Console Redirection Settings, and specify how the computer and the host computer to which are connected exchange information.

Out-of-Band Mgmt Port

Microsof t Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.

Terminal Type EMS

Use this item to select the preferred terminal emulation type for out-of-band management. It is recommended to select [VT-UTF8].

Option	Description
VT100	ASCII character set
VT100+	Extended VT100 that supports color and function keys
VT-UTF8	UTF8 encoding is used to map Unicode chars onto 1 or more bytes
ANSI	Extended ASCII character set

Bits Per Second EMS

Use this item to select the serial port transmission speed. The speed used in the host computer and the client computer must be the same. Long or noisy lines may require lower transmission speed. The options include [9600], [19200], [57600] and [115200].

Flow Control EMS

Use this item to set the flow control to prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a "stop" signal can be sent to stop the data flow. Once the buffers are empty, a "start" signal can be sent to restart the flow. Hardware flow uses two wires to send start/stop signals. The options include [None], [Hardware RTS/CTS], and [Software Xon/Xoff].

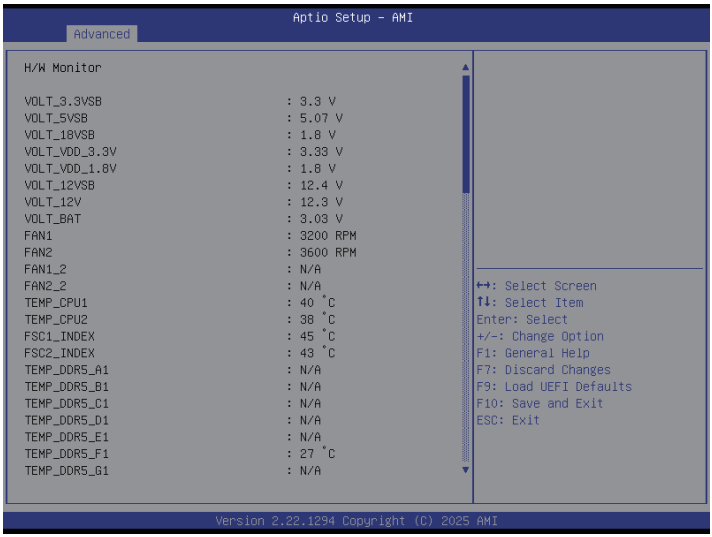
Data Bits EMS

Parity EMS

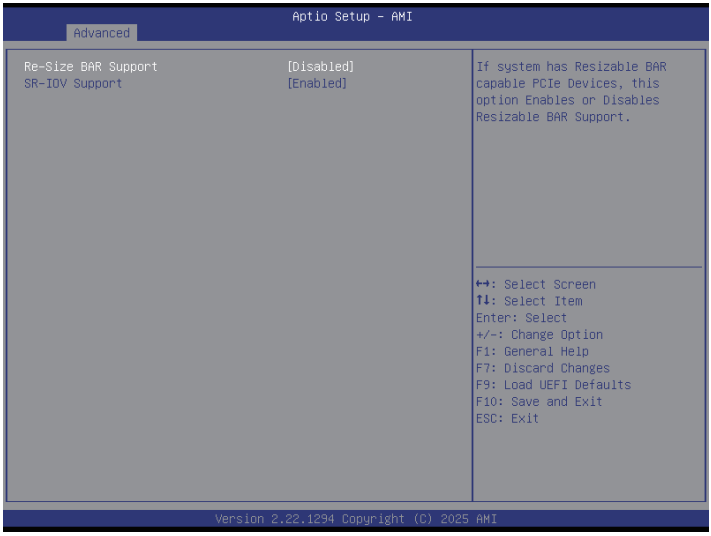
Stop Bits EMS

3.3.9 H/W Monitor

In this section, it allows user to monitor the status of the hardware on the system, including the parameters of the CPU temperature, motherboard temperature, CPU fan speed, chassis fan speed, and the critical voltage.



3.3.10 PCI Subsystem Settings



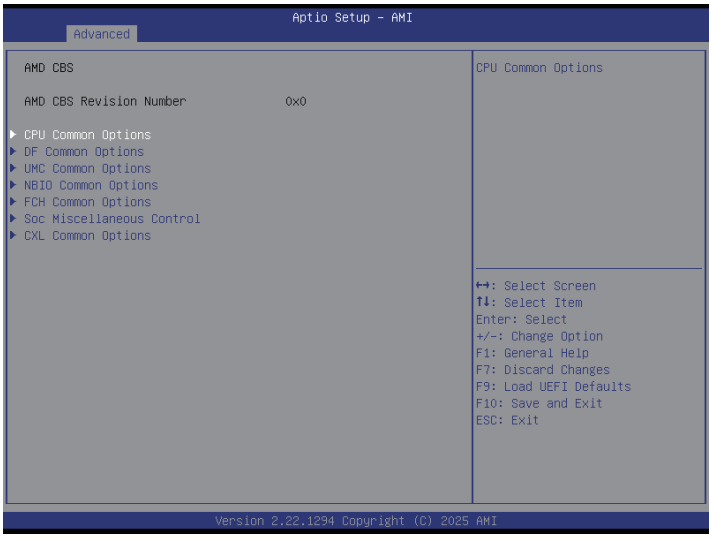
Re-Size BAR Support

If the system has Resizable BAR capable PCIe Devices, this option enalbes or disables the Resizable BAR Support.

SR-IOV Support

If the system has SR-IOV capable PCIe Devices, this option enalbes or disables the Single Root IO Virtualiztion Support.

3.3.11 AMD CBS



CPU Common Options

Use this item to configure CPU Common options.

Performance

Use this item to configure CPU performance.

REP-MOV/STOS Streaming

This item allows REP-MOVS/STOS to use non-caching streaming stores for large sizes.

Prefetcher Settings

Use this item to configure L1 Stream HW, L1 Stride, L1 Region, L2 Stream HW, L2 Up/Down and L1 Burst Prefetcher Settings.

Core Watchdog

Use this item to configure CPU Watchdog Timer.

RedirectForReturnDis

From a workaround for GCC/C000005 issue for XV Core on C2 A0, setting MSRC001_1029 Decode Configuration (DE_CFG) bit 14 [DecfgNoRdrctForReturns] to 1.

Platform First Error Handling

Use this item to enable or disable PFEH, cloak individual banks, and mask deferred error interrupts from each bank.

Core Performance Boost

Use this item to configure Core Performance Boost.

Global C-state Control
Use this item to controls IO based C-state generation and DF C-states.

Power Supply Idle Control
Use this item to configure Power Supply Idle Control.

Streaming Stores Control
Use this item to enable or disable the streaming stores functionality.

Local APIC Mode
Use this item to configure local APIC operation modes.

ACPI_CST C1 Declaration
Determines whether or not to declare the C1 state to the OS.

ACPI CST C2 Latency
Enter in microseconds (decimal value). Larger C2 latency values will reduce the number of C2 transitions and reduce C2 residency.

MCA Error Thresh Enable
Use this item to enable MCA error thresholding.

MCA Frutext
Use this item to enable or disable MCA FruText.

SMU and PSP Debug Mode
When this option is enabled, uncorrected errors detected by the PSP FW or SMU FW that should cause a cold reset, will hang and not reset the system.

PPIN Opt-in
Use this item to turn on PPIN feature.

SMEE
Use this item to control secure memory encryption enable. Enabling both SMEE and SME-MK are not supported. Results in #GP.

Action on BIST Failure
When a CCD BIST failure is detected, the action will be taken.

Enhanced REP MOVSB/STOSB (ERSM)
The Default value is 1, also can be set to zero for analysis purposes as long as OS support it.

Log Transparent Errors
Log transparent errors in MCA in addition to debug registers.

AVX512
Use this item to enable or disable AVX512.

ERMSB Caching Behavior
Enable: Optimized cashing for REPS.
Disable: Legacy caching behavior for REPs.

CPU Specuiative Store Modes

Balanced: Store instructions may delay sending out their invalidations to remote cacheline copies when the cacheline is present but not in a writable state in the local cache.

More Speculative: Store instructions will send out invalidations to remote cacheline copies as soon as possible.

Less Speculative: Store instructions may delay sending out their invalidations to remote cacheline copies when the cacheline is not present in the local cache or not in a writable state in the local cache.

Fast Short REP MOVSB (FSRM)

The Default value is 1, also can be set to zero for analysis purposes as long as OS support it.

PauseCntSe1_1_0

Number of cycles dispatch is stalled for a thread after dispatching PAUSE instruction. POR is 64 cycles.

Prefetch/Request Throttle

Enables XI logic which calculates average latency, updates throttle level, and sends throttle level messages to L2.

Scan Dump Debug Enable

This item operates like below settings (when enabled) to avoid the reset caused by Syncflood, etc.

APCB_TOKEN_UID_PSP_ENABLE_DEBUG_MODE = 1 (Enabled)

APCB_TOKEN_UID_DF_EXT_IP_SYNC_F_LOOD_PROP = 1 (Sync flood disabled)

PcdResetCpuOnSyncFlood = 0 (Disable)

MCAX 64 Bank Support

Use this item to enable 64 MCA banks per thread mapping.

Adaptive Allocation (AA)

Disable to use fixed L2 replacement/allocation policy.

Latency Under Load (LUL)

Enabling may improve latency in heavy BW scenarios. May slightly reduce peak CCD BW.

Core Trace Dump Enable

Use this item to enable or disable Core Trace Dump feauture.

FP512

Indicates support for downgrading FP512 datapathto FP256. Enable = 512bit datapath, Disable = 256bit datapath.

AMD_ERMSB Reporting

Reprot presence of AMD_ERMSB via CPUID. By default, this is reported as true (Enable), the field can be set to false for analysis purposes as long as OS supports it.

DF Common Options

Use this item to configure DF Common options.

Memory Addressing
Use this item to configure memory addressing.

ACPI
Use this item to configure ACPI.

Link
Use this item to configure Link.

SDCI
Use this item to configure Smart Data Cache Injection (SDCI) feature.

Probe Filter
Use this item to configure Probe Filter.

DF Watchdog Timer Interval
Use this item to configure the Data Fabric watchdog timer interval.

Disable DF to external IP SyncFloodPropagation
Use this item to disable SyncFlood to UMC & downstream slaves.

Sync Flood Propagation to DF Components
Use this item to configure Sync Flood Propagation to DF Components.

Freeze DF Module Queues on Error
Use this item to configure Freeze DF Module Queues on Error.

CC6 Memory Region Encryption
Use this item to control whether or not the CC6 save/restore memory is encrypted.

CCD B/W Balance Throttle Level
Use this item to enable throttling of memory traffic per CCD. Increased throttling can reduce imbalance across CCDs (expected to be rare).

Number of PCI Segments
Use this item to configure Number of PCI Segments.

CCM Throttler
Use this item to limit peak CCM throughput.

Clean Victim FTI Cmd Balancing
Use this item to control Clean Victim FTI Cmd Balancing feature.

CXL Strongly Ordered Writes
Determines how the host treats Strongly ordered Writes (ItoMWr and MemWr) from CXL. cache devices.

UMC Common Options

Use this item to configure UMC Common options including DDR Addressing Options, DDR Controller Configuration, DDR MBIST Options, DDR RAS, DDR Bus Configuration, DDR Timing Configuration, DDR Training Options, DDR Security, DDR PMIC Configuration, DDR Thermal Throttling and DDr Miscellaneous.

NBIO Common Options

Use this item to configure NBIO Common options.

SMU Common Options
Use this item to configure SMU Common Options.

NBIO RAS Common Options
Use this item to configure NBIO RAS Common Options.

PCIE
Use this item to configure PCIE.

nBif Common Options
Use this item to configure nBif Common Options.

IOMMU/Security
Use this item to configure IOMMU/Security.

Enable Port Bifurcation
Use this item to configure Enable Port Bifurcation.

Link EQ Preset Options
Use this item to configure Link EQ Preset Options.

PCIe Loopback Mode
Use this item to enable or disable PcieLoopBackMode.

Enable 2 SPC (Gen 4)
Enable this setting to use 2 symbols per clock for devices at Gen 4 speed.

Enable 2 SPC (Gen 5)
Enable this setting to use 2 symbols per clock for devices at Gen 5 speed.

Safe Recovery upon a BERExceeded Error
Use this item to configure Safe Recovery upon a BERExceeded Error.

Periodic Callbration
Use this item to configure Periodic Callbration.

FCH Common Options

Use this item to configure FCH Common options including I3C/I2C Configuration Options, SATA Configuration Options, USB Configuration Options, Ac Power Loss Options, Uart Configuration Options, FCH RAS Options and Miscellaneous Options.

Soc Miscellaneous Control

Use this item to configure Soc Miscellaneous Control options.

ABL Console Out Control
Enable: Enable ConsoleOut Funciton for ABL.
Disable: Disable ConsoleOut Funciton for ABL.
Auto: Keep default behavior.

ABL Console Out Serial Port
eSPI UART: Enable serial port through eSPU UART.
SOC UARTO: Enable serial port through SOC UART0.
SOC UART1: Enable serial port through SOC UART1.
Auto: Keep default behavior.

ABL Console Out Serial Port IO
Select Legacy Uart (SIO or eSPI) IO base.
0x3F8: Set IO base to 0x3F8
0x2F8: Set IO base to 0x2F8
0x3E8: Set IO base to 0x3E8
0x2E8: Set IO base to 0x2E8
Auto: Keep default behavior.

ABL Serial Port IO Customized Enabled
Use this item to configure ABL Serial Port IO Customized Enabled.

ABL Basic Console Out Control
Enable: Enable Basic ConsoleOut Funciton for ABL.
Disable: Disable Basic ConsoleOut Function for ABL.
Auto: Keep default behavior.

ABL PMU Message Control
Use this item to control the total number of PMU debug message.

ABL Memory Population Message Control
Non-Recommended configurations may be functional but may not be validated by AMD. Select 'warning message': To show warning messages if Memory channel configuration does NOT follow Memory Population Guidelines. 'Fatal error': To show the messages and halt the system.

Print Socket 1 PMU MsgBlock
Print Socket 1 PMU MsgBlock contents after training.

Print Socket 1 PMU Training Log
Print Socket 1 PMU training log while 'ABL PMU message Control' == Detailed debug message.

SP Error Injection Support
Use this item to enable EINJ support.
Set this item [True] to enable EINJ support.

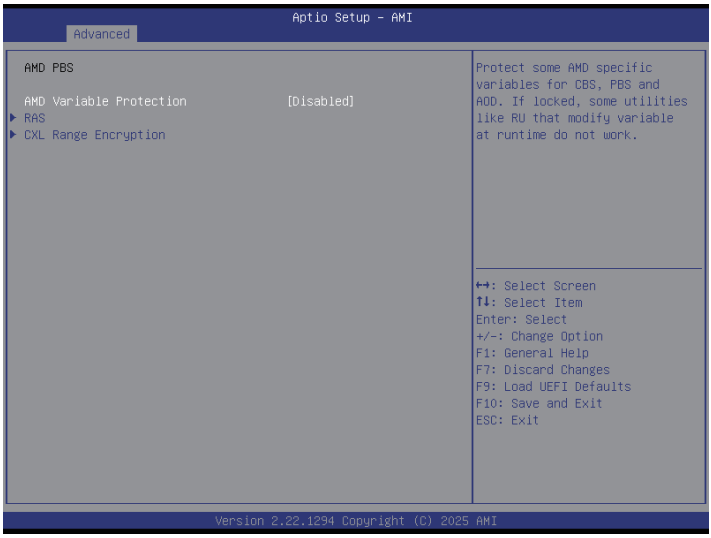
Firmware Anti-rollback (FAR)
Use this item to configure Firmware Anti-rollback (FAR).

SEC_I2C Voltage Mode
Use this item to configure SEC_12C Voltage Mode.

CXL Common Options

Use this item to configure CXL Common options including CXL Control, CXL Physical Addressing, CXL Memory Attribute, CXL Encryption, CXL DVSEC Lock, CXL HDM Decoder Lock On Commit, Temp Gen5 Advertisement, Sync Header Bypass, Sync Header Bypass Compatibility Mode, CXL RAS, CXL Memory Online/Offline and Override CXL Memory Size.

3.3.12 AMD PBS



AMD Variable Protection

Enable to protect some AMD specific variables for CBS, PBS and ADD. If locked, some utilities like RU that modify vaiable at runtime do not work.

RAS

Use this item to configure AMD CPM RAS related settings.

RAS Periodic SMI Control
Use this to enable or disable Periodic SMI for polling [MCA Threshold] error.

SMI Threshold
This limits the number of [MCA Threshold and Deferred Error SMI source] per a unit time.

SMI Scale
Use this to define the time scale.

SMI Scale Unit
Use this to define the unit of time scale.

SMI Period
Use this to define the polling interval with ms unit. Input 0 value to disable this function.

GHES Notify Type
This specifies the notification type for deferred/corrected errors.

GHES UnCorr Notify Type
This specifies the notification type for uncorrected errors.

PCIe GHES Notify Type
This specifies the notification type for PCIe corrected errors.

PCIe UnCorr GHES Notify Type
This specifies the notification type for PCIe uncorrected errors.

PCIe Root Port Corr Err Mask Reg
Use this to initialize the PCIe AER Corrected Error Mask register of root port.

PCIe Root Port UnCorr Err Mask Reg
Use this to initialize the PCIe AER Uncorrected Error Mask register of root port.

PCIe Root Port UnCorr Err Sev Reg
Use this to initialize the PCIe AER Uncorrected Error Severity registers of root port.

PCIe Device Corr Err Mask Reg
Use this to initialize the PCIe AER Corrected Error Mask register of PCIe device.

PCIe Device UnCorr Err Mask Reg
Use this to initialize the PCIe AER Uncorrected Error Mask register of PCIe device.

PCIe Device UnCorr Error Sev Reg
Use this to initialize the PCIe AER Uncorrected Error Severity registers of PCIe device

CXL DP CIE Mask Enable
Use this to enable or disable masking of CXL DP Correctable Error-Internal Error.

DRAM Hard Post Package Repair
Use this to enable or disable the spare DRAM rows to replace malfunctioning rows via an in-field repair mechanism.

HEST DMC Structure Support
Use this to enable or disable HEST DMC (Deffered Maching Check) Structure Support.

CXL Error Report Support
Use this to enable or disable CXL Error Reporting.

CXL Range Encryption

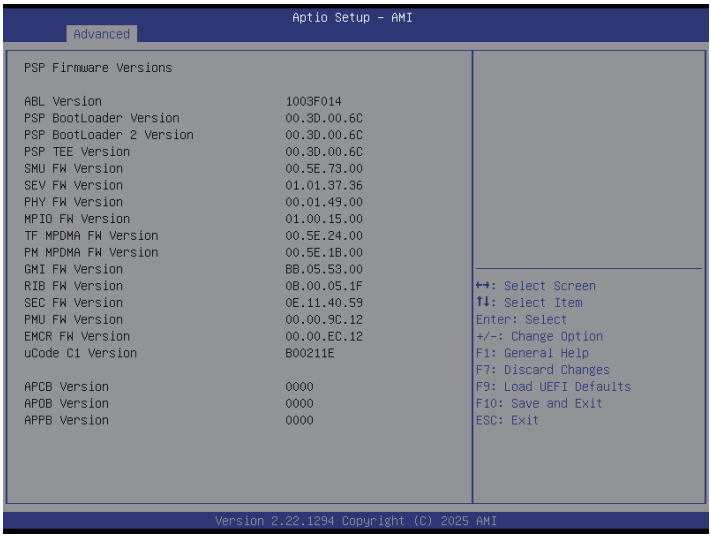
Configure AMD CXL range encryption setting.

Range 1/2/3/4/5/6/7 Memory Base
This item allows user to enter memory range base address.

Range 1/2/3/4/5/6/7 Memory Limit
This item allows user to enter memory range limit address.

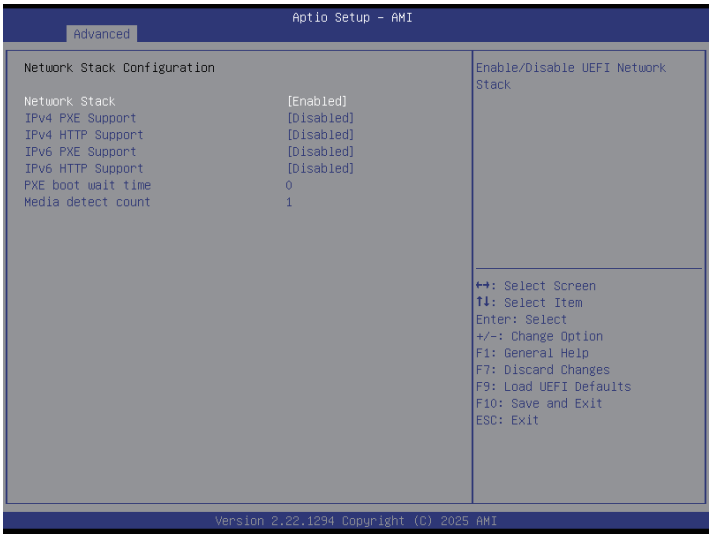
Start CXL Range Encryption
Use this to encrypt all memory ranges..

3.3.13 PSP Firmware Versions



The PSP Firmware Verions displays the version information of ABL, PSP BootLoader, PSP BootLoader 2, PSP TEE, SMU FW, SEV FW, PHY FW, MPIO FW, TF MPDMA FW, PM MPDMA FW, GMI FW, RIB FW, SEC FW, PMU FW, EMCR FW, uCode C1, APCB, APOB and APPB.

3.3.14 Network Stack Configuration



Network Stack

Use this to enable or disable UEFI Network Stack.

IPv4 PXE Support

Use this to enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

IPv4 HTTP Support

Use this to enable or disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.

IPv6 PXE Support

Use this to enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

IPv6 HTTP Support

Use this to enable or disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.

PXE boot wait time

Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

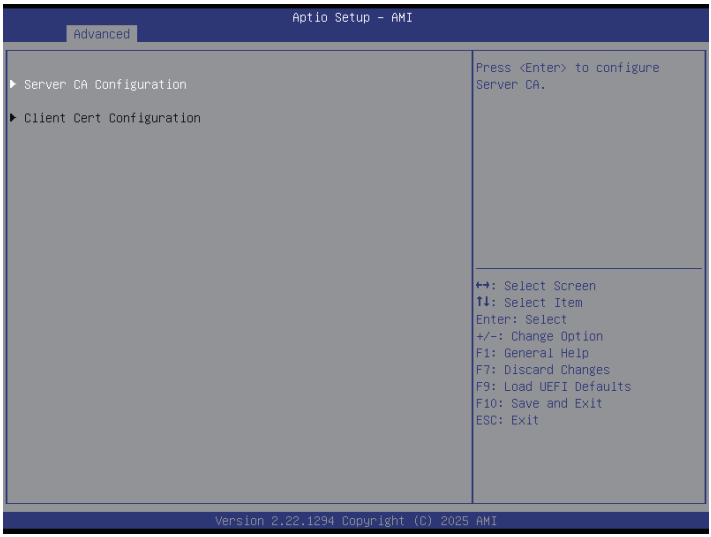
Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

3.3.15 Driver Health

Inter (R) PRO/1000 7.4.36 PCI-E Healthy

Provides Health Status for the Drivers/Controllers

3.3.16 Tls Auth Configuration



Server CA Configuration

Press <Enter> to configure Server CA.

Client Cert Configuration

Enroll Cert

Press <Enter> to enroll cert.

Delete Cert

Press <Enter> to delete cert.

3.3.17 Instant Flash

Instant Flash is a UEFI flash utility embedded in Flash ROM. This convenient UEFI updatetool allows user to update system UEFI without entering operating systems first like MSDOS or Windows®. Just save the new UEFI file to the USB flash drive, floppy disk or hard drive and launch this tool, then update the UEFI only in a few clicks without preparing an additional floppy diskette or other complicated flash utility. Please be noted that the USB flash drive or hard drive must use FAT32/16/12 file system. Execute the Instant Flash utility, the utility will show the UEFI files and the respective information. Select the proper UEFI file to update UEFI, and reboot the system after the UEFI update process is completed.

3.4 Server Mgmt

Wait For BMC

Wait For BMC response for specified time out. BMC starts at the same time when BIOS starts during AC power ON. It takes around 255 seconds to initialize Host to BMC interfaces.

FRB-2 Timer

Use this item to enable or disable FRB-2 timer (POST timer)

FRB-2 Timer Timeout

Use this to define the FRB-2 Time Expiration between 1 to 30 value.

FRB-2 Timer Policy

Configure how the system should respond. If the FRB-2 Timer expires is disabled, this item is not available.

OS Watchdog Timer

Use this item to enable or disable OS Watchdog Timer. If enabled, starts a BIOS timer which can only be shut off by Management Software after the OS loads.

OS Wtd Timer Timeout

Configure the OS Boot Watchdog Timer Expiration between 1 to 30 min value. If the OS Boot Watchdog Timer is disabled, this item is not available.

OS Wtd Timer Policy

Configure how the system should respond if the OS Boot Watchdog Timer expires. If the OS Boot Watchdog Timer is disabled, this item is not available.

BMC Network Configuration

Use this to configure BMC network parameters.

DNS Configuration

Use this to configure DNS parameters.

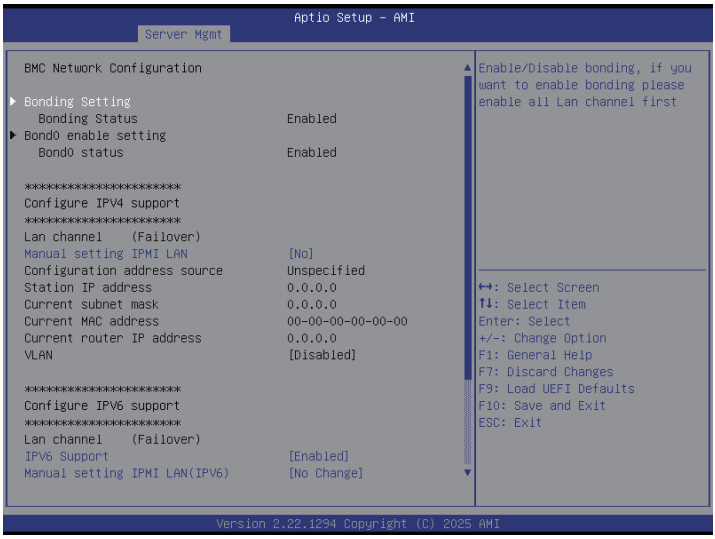
System Event Log

Press <Enter> to change the SEL event log configuration.

BMC Tools

Use this item to configure about KCS control, restore AC power loss and load BMC default setings.

3.4.1 BMC Network Configuration



Bonding Setting

Select this item to enabled or disabled bonding. Please enable all lan channel first when want to enable bonding.

Manual Setting IPMI LAN

If [No] is selected, the IP address is assigned by DHCP. If using a static IP address, toggle to [Yes], and the changes take effect after the system reboots. The default value is [No].

Configuration Address Source

Select to configure BMC network parameters statically or dynamically(by BIOS or BMC). Configuration options: [Static] and [DHCP].

Static: Manually enter the IP Address, Subnet Mask and Gateway Address in the BIOS for BMC LAN channel configuration.
DHCP: IP address, Subnet Mask and Gateway Address are automatically assigned by the network's DHCP server.

The default login information for the IPMI web interface is:
Username: admin
Password: admin

For more instructions on how to set up remote control environment and use the IPMI management platform, please refer to the IPMI Configuration User Guide or go to the Support website at: http://www.asrockrack.com/support/faq.asp

VLAN

Enable or disable Virtual Local Area Network.

If [Enabled] is selected, configure the items below.
VLAN ID: Select this item to configure the VLAN ID setting, the Maximum value is 4094 and the Minimum value is 1.
VLAN Priority: Select this item to configure the VLAN Priotity setting. the Maximum value is 7 and the Minimum value is 0.

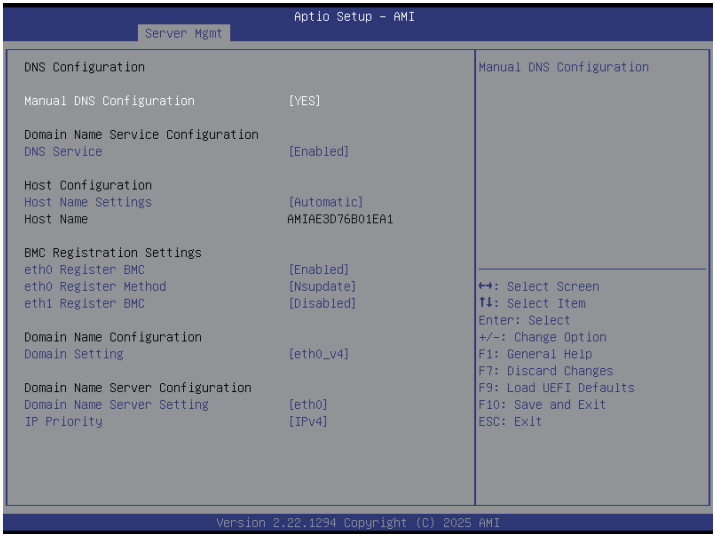
IPV6 Support

Enable or disable LAN IPV6 Support.

Manual Setting IPMI LAN(IPV6)

Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.

3.4.2 DNS Configuration



Manual DNS Configuration

Select this item to manual configure DNS.

If [YES] is selected, configure the items below.

DNS Service

Select this item to enable or disable DNS Service Configuration.

Host Name Settings

Select this item to automatic or manual Host Name Settings.

eth0 Register BMC

Select this item to enable or disable Register BMC.

eth0 Register Method

Select this item to configure Register Method with Nsupdate or DHCP client FQDN/ Hostname.

eth1 Register BMC

Select this item to enable or disable Register BMC.

eth1 Register Method

Select this item to configure Register Method with Nsupdate or DHCP client FQDN/ Hostname.

Domain Setting

This item supports Manual, Bond0_v4 and Bond0_v6 Domain Settings.

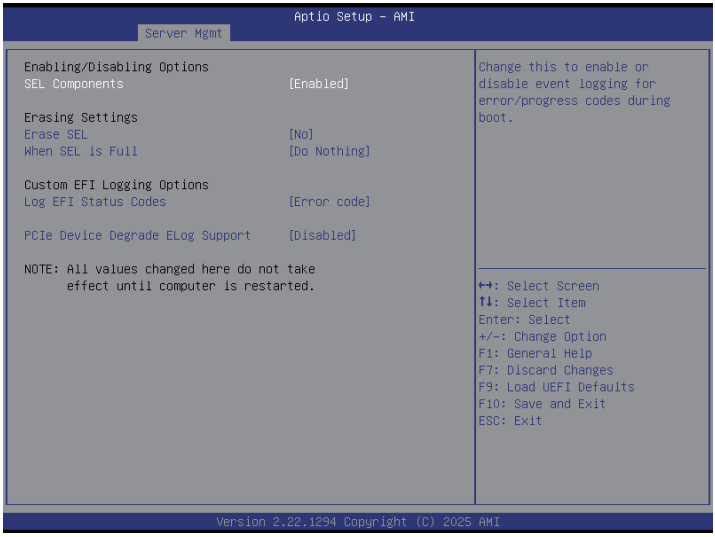
Domain Name Server Setting

Select this item to configure DNS Server Settings Manual/ethx.

IP Priority

Select this item to configure IP Priority IPV4/IPV6.

3.4.3 System Event Log



SEL Components

Change this to enable or disable event logging for error/progress codes during boot.

Erase SEL

Use this to choose options for earsing SEL.

When SEL is Full

Use this to choose options for reactions to a full SEL.

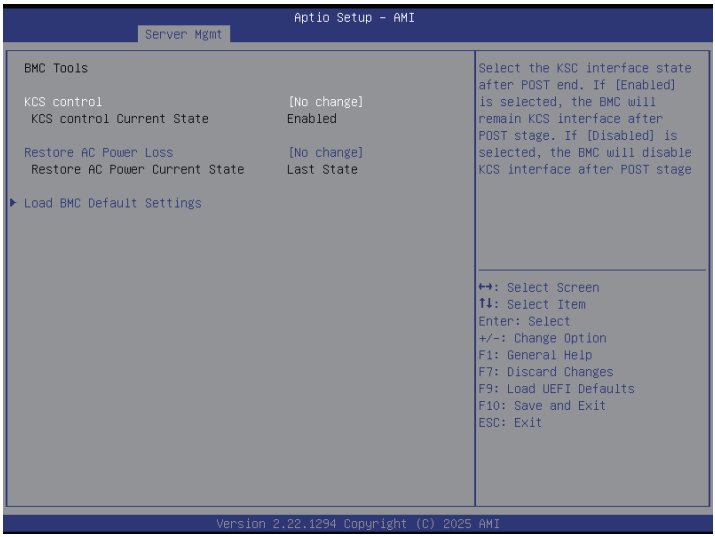
Log EFI Status Codes

Use this item to disable the logging of EFI Status Codes or log only error code or only progress code or both.

PCIe Device Degrade ELog Support

Use this item to enable or disable PCIe Device Degrade Error Logging Support.

3.4.4 BMC Tools



KCS Control

Select this KCS interface state after POST end. If [Enabled] us selected, the BMC will remain KCS interface after POST stage. If [Disabled] is selected, the BMC will disable KCS interface after POST stage

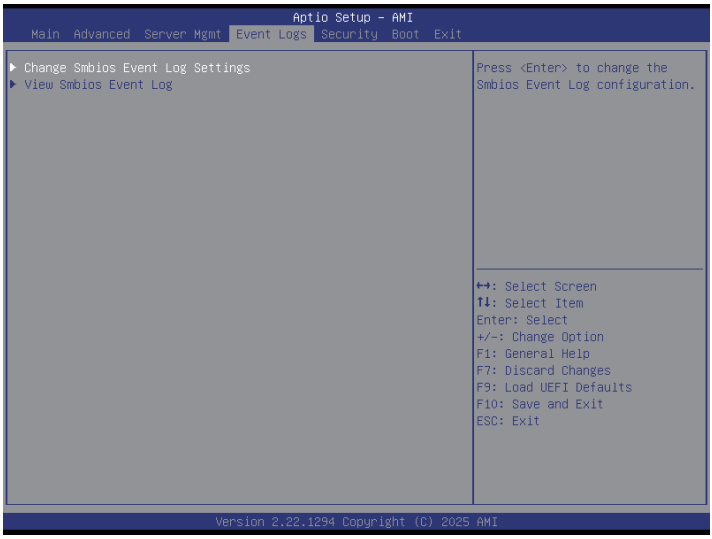
Restore AC Power Loss

This allows user to set the power state after an unexpected AC/power loss. If [Power Off] is selected, the AC/power remains off when the power recovers. If [Power On] is selected, the AC/power resumes and the system starts to boot up when the power recovers. If [Last State] is selected, it will recover to the state before AC/power loss.

Load BMC Default Settings

Use this item to Load BMC Default Settings

3.5 Event Logs



Change Smbios Event Log Settings

Use this item to configure the Smbios Event Log Settings.
When entering the item, the screen displays following sub-items:

Smbios Event Log
Use this item to enable or disable all features of the SMBIOS Event Logging during system boot.

Erase Event Log
Choose options for erasing Smbios Event Log. Erasing is done prior to any logging activation during reset.

When Log is Full
Use this item to choose options for reactions to a full Smbios Event Log. The options include [Do Nothing] and [Erase Immediately].

Log System Boot Event
Choose option to enable/disable logging of System boot event.

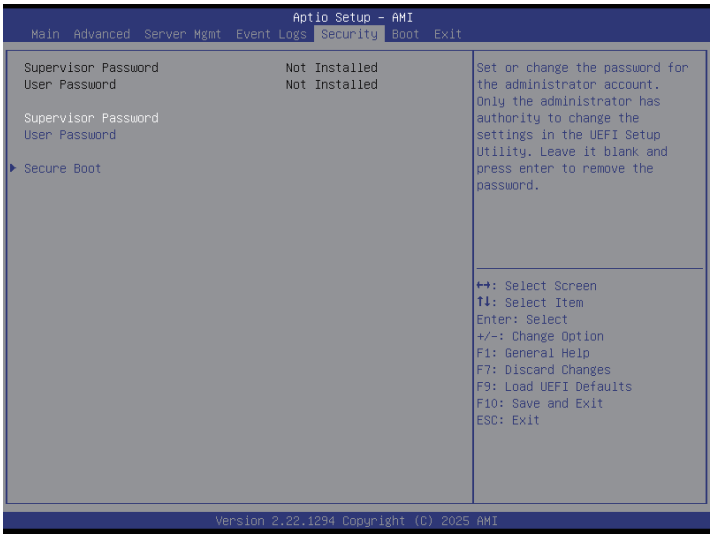
View Smbios Event Log

Press <Enter> to view the Smbios Event Log records.

All values changed here do not take effect until computer is restarted.

3.6 Security

This section allows user to set or change the supervisor/user password for the system. For the user password item is allowed user to clear it.



Supervisor Password

Set or change the password for the administrator account. Only the administrator has authority to change the settings in the UEFI Setup Utility. Leave it blank and press enter to remove the password.

User Password

Set or change the password for the user account. Users are unable to change the settings in the UEFI Setup Utility. Leave it blank and press enter to remove the password.

Secure Boot

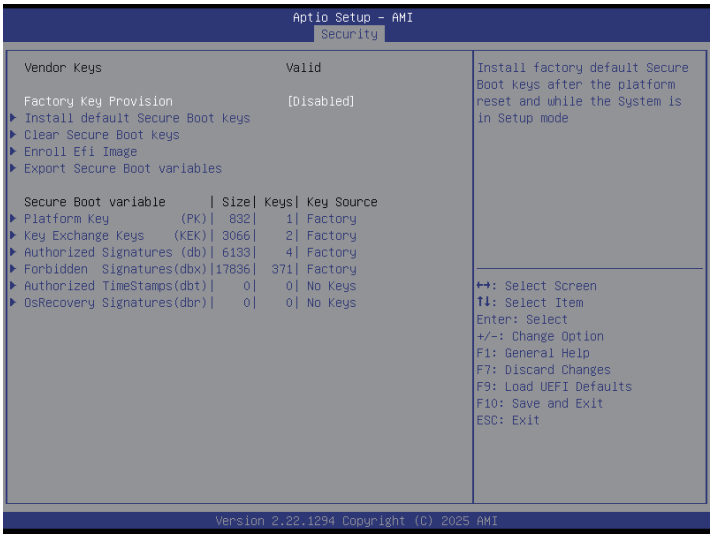
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key(PK) is enrolled and the System is in User mode. The mode change requires platform reset.

Secure Boot Mode

Secure Boot mode selector: Standard/Custom. In Custom mode Secure Boot Variables can be configured without authentication.

3.6.1 Key Management

In this section, expert users can modify Secure Boot Policy variables without full authentication.



Factory Key Provision

Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode.

Install Default Secure Boot Keys

Please install default secure boot keys if it's the first time to use secure boot.

Clear Secure Boot Keys

This force system to setup Mode-Clear all Secure Boot Variables. Change takes effect after reboot.

Enroll Efi Image

Allow the image to run in Secure Boot mode. Enroll SHA256 hash of the binary into Authorized Signature Database (db).

Export Secure Boot Variables

Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device.

Platform Key (PK)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

Key Exchange Keys (KEK)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

Authorized Signatures (db)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

Forbidden Signatures (dbx)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

Authorized TimeStamps (dbt)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

OsRecovery Signatures (dbr)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

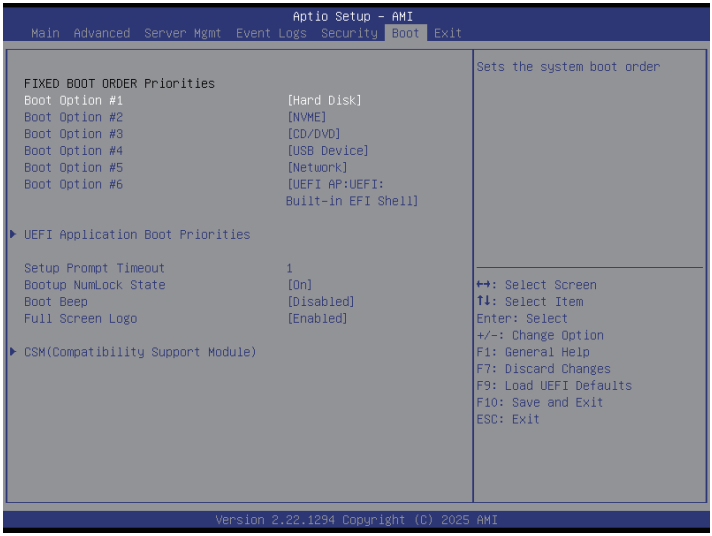
2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

3.7 Boot Screen

In this section, it will display the available devices on the system for user to configure the boot settings and the boot priority.



Boot Option #1/#2/#3/#4/#5/#6

Use this to set the system boot order.

UEFI Application Boot Priorities

Specifies the Boot Device Priority sequence from available UEFI Application.

Setup Prompt Timeout

Configure the number of seconds to wait for the UEFI setup utility.

Bootup NumLock State

Select whether Num Lock should be turned on or off when the system boots up.

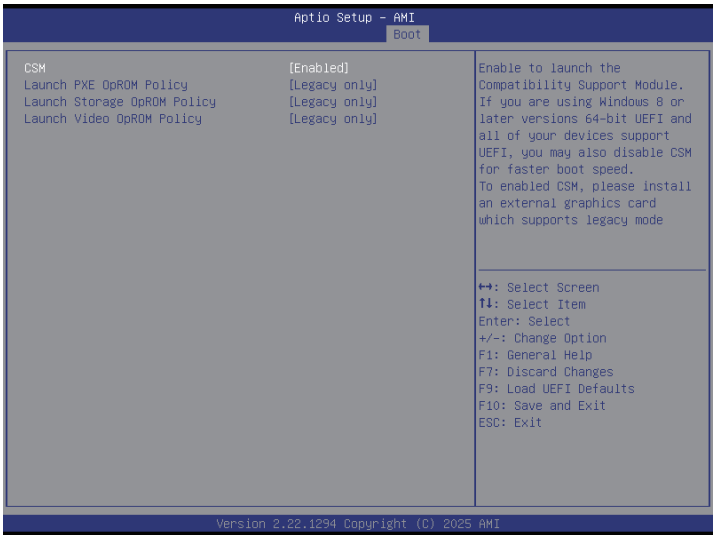
Boot Beep

Select whether the Boot Beep should be turned on or off when the system boots up. Please note that a buzzer is needed.

Full Screen Logo

Enable to display the boot logo or disable to show normal POST message.

3.7.1 CSM Parameters



CSM (Compatibility Support Module)

CSM

Select this item to enable or disable the Compatibility Support Module. Please do not disable unless running a WHCK test. For faster boot speed, it may also disable CSM. To enabled CSM, please install an external graphics card which supports legacy mode.

Launch PXE OpROM Policy

Select UEFI only to run those that support UEFI option ROM only. Select Legacy only to run those that support legacy option ROM only. Select Do not launch to not execute both legacy and UEFI option ROM.

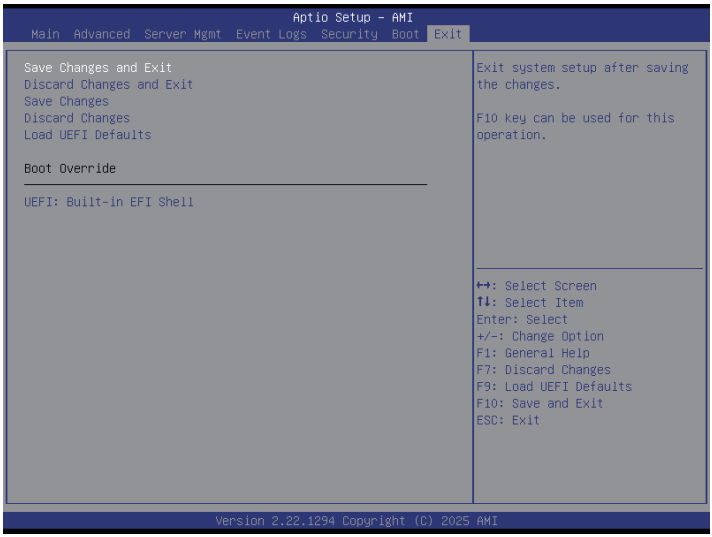
Launch Storage OpROM Policy

Select UEFI only to run those that support UEFI option ROM only. Select Legacy only to run those that support legacy option ROM only. Select Do not launch to not execute both legacy and UEFI option ROM.

Launch Video OpROM Policy

Select UEFI only to run those that support UEFI option ROM only. Select Legacy only to run those that support legacy option ROM only. Select Do not launch to not execute both legacy and UEFI option ROM.

3.8 Exit Screen



Save Changes and Exit

When selecting this option, the following message “Save configuration changes and exit setup?” will pop-out. Press <F10> key or select [Yes] to save the changes and exit the UEFI SETUP UTILITY.

Discard Changes and Exit

When selecting this option, the following message “Discard changes and exit setup?” will pop-out. Press <ESC> key or select [Yes] to exit the UEFI SETUP UTILITY without saving any changes.

Save Changes

When selecting this option, the following message “Save changes?” will pop-out. Select [Yes] to save all changes.

Discard Changes

When selecting this option, the following message “Discard changes?” will pop-out. Select [Yes] to discard all changes.

Load UEFI Defaults

Use this item to restore or load default values for all the setup options.

Chapter 4 Software Support

After all the hardware has been installed, it suggests to go to the offical website at http://www.ASRockRack.com and make sure if there are any new updates of the BIOS / BMC firmware for the motherboard.

4.1 Download and Install Operating System

This motherboard supports various Microsoft® Windows® Server / Linux compliant operating systems. Please download the operating system from the OS manufacturer. Please refer to the OS documentation for more instructions.

4.2 Download and Install Software Drivers

This motherboard supports various Microsoft® Windows® compliant drivers. Please download the required drivers from the website at http://www.ASRockRack.com.

To download necessary drivers, go to the product page, click on the "Download" tab, choose the operating system that is used, and then download the using driver.

Chapter 5 Troubleshooting

5.1 Troubleshooting Procedures

Follow the procedures below to troubleshoot the system.

Always unplug the power cord before adding, removing or changing any hardware components. Failure to do so may cause physical injuries and damages to motherboard components.

1. Disconnect the power cable and check whether the PWR LED is off.
2. Unplug all cables, connectors and remove all add-on cards from the motherboard. Make sure that the jumpers are set to default settings.
3. Confirm that there are no short circuits between the motherboard and the chassis.
4. Install a CPU and fan on the motherboard, then connect the chassis speaker and power LED.

If there is no power...

1. Confirm that there are no short circuits between the motherboard and the chassis.
2. Make sure that the jumpers are set to default settings.
3. Check the settings of the 115V/230V switch on the power supply.
4. Verify if the battery on the motherboard provides ~3VDC. Install a new battery if it does not.

If there is no video...

1. Try replugging the monitor cables and power cord.
2. Check for memory errors.

If there are memory errors...

1. Verify that the DIMM modules are properly seated in the slots.
2. Use recommended DDR5 RDIMM/RDIMM-3DS.
3. Install more than one DIMM modules that should be identical with the same brand, speed, size and chip-type.
4. Try inserting different DIMM modules into different slots to identify faulty ones.
5. Check the settings of the 115V/230V switch on the power supply.

Unable to save system setup configurations...

1. Verify if the battery on the motherboard provides ~3VDC. Install a new battery if it does not.
2. Confirm whether the power supply provides adaquate and stable power.

Other problems...

1. Try searching keywords related to the related problem on ASRock Rack's FAQ page: http://www.asrockrack.com/support

5.2 Technical Support Procedures

If the problems are still unsolved, please contact ASRock Rack's technical support with the following information:

1. Contact information
2. Model name, BIOS version and problem type.
3. System configuration.
4. Problem description.

Contact ASRock Rack's technical support at:
http://www.asrockrack.com/support/tsd.asp

5.3 Returning Merchandise for Service

For warranty service, the receipt or a copy of the invoice marked with the date of purchase is required. By calling the vendor or going to RMA website (http://event. asrockrack.com/tsd.asp) to obtain a Returned Merchandise Authorization (RMA) number.

The RMA number should be displayed on the outside of the shipping carton which is mailed prepaid or hand-carried when returning the motherboard to the manufacturer. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty does not cover damages incurred in shipping or from failure due to alteration, misuse, abuse or improper maintenance of products.

Contact the distributor first for any product related problems during the warranty period.

Contact Information

If it needs to contact ASRock Rack or want to know more about ASRock Rack, you're welcome to visit ASRock Rack's website at http://www.asrockrack.com; or contact the dealer for further information. For technical questions, please submit a support request form at https://event.asrockrack.com/tsd.asp

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