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Server/Workstation
Motherboard

GNRAP2D24G-2L+

User Manual

English



Version 1.00

Published Aug. 2026

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This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) this device may not cause harmful interference, and
- (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.



ASRock Rack INC. hereby declares that this device is in compliance with the essential requirements and other relevant provisions of related Directives. Full text of EU declaration of conformity is available at: <http://www.asrockrack.com>

ASRock Rack follows the green design concept to design and manufacture our products, and makes sure that each stage of the product life cycle of ASRock Rack product is in line with global environmental regulations. In addition, ASRock Rack disclose the relevant information based on regulation requirements.

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DO NOT throw the motherboard in municipal waste. This product has been designed to enable proper reuse of parts and recycling. This symbol of the crossed out wheeled bin indicates that the product (electrical and electronic equipment) should not be placed in municipal waste. Check local regulations for disposal of electronic products.

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Chapter 1 Introduction

Thank you for purchasing ASRock Rack **GNRAP2D24G-2L+** motherboard, a reliable motherboard produced under ASRock Rack's consistently stringent quality control. It delivers excellent performance with robust design conforming to ASRock Rack's commitment to quality and endurance.

In this manual, chapter 1 and 2 contains introduction of the motherboard and step-by-step guide to the hardware installation. Chapter 3 and 4 contains the configuration guide to BIOS setup and information of the software support.



Because the motherboard specifications and the BIOS software might be updated, the content of this manual will be subject to change without notice. In case any modifications of this manual occur, the updated version will be available on ASRock Rack website without further notice. Find the latest memory and CPU support lists on ASRock Rack website as well. ASRock Rack's Website: www.ASRockRack.com

*Please visit the website for specific information and technical support:
<http://www.asrockrack.com/support/>*

1.1 Package Contents

- ASRock Rack GNRAP2D24G-2L+ motherboard
(Proprietary form factor: 16.93" x 15.17", 430 mm x 385.35 mm)
- Quick installation guide
- 1 I/O shield
- 1 ATX 4P to 24P power cable (8 cm)
- 2 Screws for M.2 sockets
- 2 CPU Non-Fabric carriers



If any items are missing or appear damaged, contact your authorized dealer.

1.2 Specifications

GNRAP2D24G-2L+	
Physical Status	
Form Factor	Proprietary
Dimension	16.93" x 15.17" (430 mm x 385.35 mm)
Processor System	
CPU	Supports Intel® Xeon® 6900E+/6900P-series processors
Socket	1+1 Socket BR (LGA 7529)
Chipset	System on Chip
System Memory	
Supported DIMM Quantity	12 + 12 DIMM slots (1DPC)
Supported Type	DDR5 RDIMM, RDIMM-3DS, MRDIMM
Max. Capacity per DIMM	RDIMM: 128 GB RDIMM-3DS: 256 GB MRDIMM: 256 GB
Max. DIMM Frequency	RDIMM: 6400 MT/s RDIMM-3DS: 6400 MT/s MRDIMM: 8800 MT/s
Voltage	1.1V
<i>Note: Memory support is to be validated.</i>	
Other PCIe Expansion Connectors	
M.2	1 M-key (PCIe5.0 x4/x2*), supports 2280/22110 form factor [CPU1] 1 M-key (PCIe5.0 x4), supports 2280/22110 form factor [CPU1] <i>*M2_1 only supports PCIe5.0 x2 when RDS2 is linked to NVSwitch.</i>
Others	10 MCIO (PCIe5.0/CXL2.0** x8) [CPU1] 12 MCIO (PCIe5.0/CXL2.0** x8) [CPU2] <i>**Up to 4 CXL devices supported per socket; CXL memory function only supported at PCIe x16 bifurcation.</i>
Ethernet	
Additional Ethernet Controller	2 RJ45 (1 GbE) by Intel® i350
Server Management	
BMC Controller	ASPEED AST2600: IPMI2.0 with iKVM and vMedia support
Dedicated IPMI LAN	1 Realtek RTL8211F for dedicated management LAN
Graphics	
Controller	ASPEED AST2600: 1 DBI5 (VGA), 1 (15-pin) header

Rear I/O	
UID Button/LED	1 UID button w/ LED
Other Button/LED	1 PWR button w/ LED, 1 RST button, 1 NMI button 1 HDD LED, 1 SYS LED
Video Port	1 DB15 (VGA)
USB Port	4 Type-A (USB 3.2 Gen1)
LAN Port	2 RJ45 (1 GbE), 1 dedicated IPMI
Internal Connectors/Headers	
Power Connector	8 Micro-Hi (8-pin, ATX 12V), 1 Micro-Fit (4-pin, ATX PSU signal) w/ ATX 24-pin adapter cable, 1 Micro-Fit (2-pin, 5V)
Auxiliary Panel Header	1 (18-pin): chassis intrusion, system fault LED, LAN activity LEDs, locate, SMBus
System Panel Connector	1 (9-pin): power switch, reset switch, system power LED, HDD activity LED
COM Header	1 (9-pin)
VGA Header	1 (15-pin)
Fan Header	6 (6-pin)
TPM Header	1 (13-pin, SPI)
VROC Header	1
HSBP	2
SMBus Header	3
PMBus Header	1
IPMB Header	1
NMI Header	1
Clear CMOS	1 (contact pads)
USB Header	1 (19-pin, 2 USB 3.2 Gen1)
Others	1 NCSI header, 1 LAN speed LED header, 1 IPMI LED header, 1 LCM header
LED Indicators	
Standby Power LED	1 (+3VSB)
80 Debug Port LED	1
Fan Fail LED	6
BMC Heartbeat LED	1
Others	1 CPLD Heartbeat LED, 1 Caterr LED, 8 CPLD Power-on Status LEDs
System BIOS	
Type	AMI UEFI BIOS: 512 Mb SPI Flash ROM
Features	Plug and Play, ACPI 4.0 (and above) compliance wake-up events, SMBIOS 3.4 and above , ASRock Rack Instant Flash
Hardware Monitor	
Temperature	CPU, MB Inlet/Outlet, M.2, RAM, i350 LAN chip temperature sensing

Fan	Fan tachometer CPU quiet fan (Allow chassis fan speed auto-adjust by CPU temperature.) Fan multi-speed control
Voltage	PVCCD_HV_CPU1/CPU2, PVCCFA_EHV_FIVRA_CPU1/CPU2, PVCCINF_CPU1/CPU2, PVCCIN_CPU1/CPU2, PVCCFA_EHV_CPU1, PVNN_TERM_CPU1, PVCC3V3_AUX_CPU1, +BAT, +3.3V, +12V, +3VSB, +5VSB
Support OS	
OS	Microsoft® Windows*: - Server 2022 (64 bit) - Server 2025 (64 bit) Linux*: - Red Hat Enterprise Linux Server 9.4 (64 bit) / 10.0 (64 bit) - SUSE Enterprise Linux Server 15 SP6 (64 bit) / 16.0 (64 bit) - Ubuntu 24.10 (64 bit) Hypervisor: - VMWare® ESXi / 8.0U3e * Ubuntu Server support RAID Mode. * Please refer to the website for the latest OS support list.
Enviroment	
Temperature	Operating temperature: 10°C ~ 35°C Non operating temperature: -40°C ~ 70°C
Humidity	Non operating humidity: 20% ~ 90% (non-condensing)

NOTE: Please refer to the website for the latest specifications.



This motherboard supports Wake from on Board LAN. To use this function, please make sure that the "Wake on Magic Packet from power off state" is enabled in Device Manager > Intel® Ethernet Connection > Power Management. And the "PCI Devices Power On" is enabled in UEFI SETUP UTILITY > Advanced > ACPI Configuration. After that, onboard LAN1&2 can wake up S5 under OS.

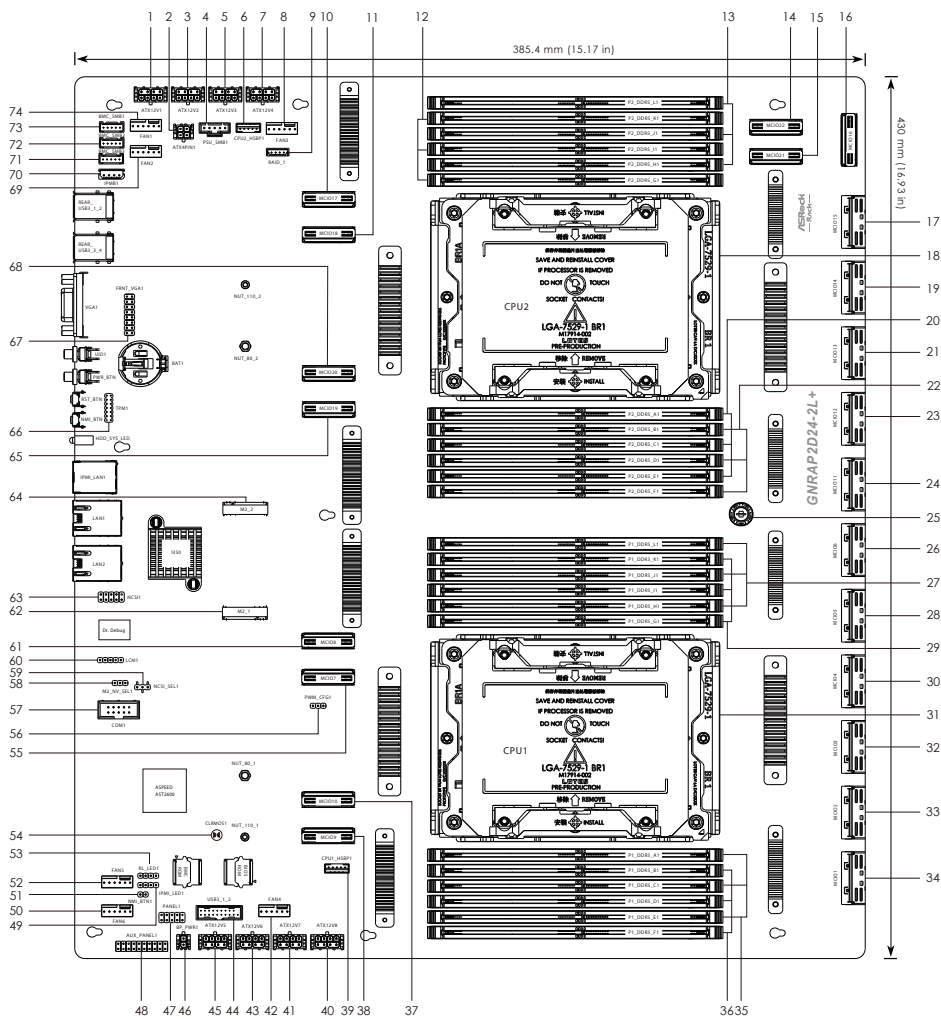


If installing Intel® LAN utility or Marvell SATA utility, this motherboard may fail Windows® Hardware Quality Lab (WHQL) certification tests. If installing the drivers only, it will pass the WHQL tests.

1.3 Unique Features

ASRock Rack Instant Flash is a BIOS flash utility embedded in Flash ROM. This convenient BIOS update tool allows you to update system BIOS without entering operating systems first like MS-DOS or Windows®. With this utility, you can press the <F6> key during the POST or the <F2> key to enter into the BIOS setup menu to access ASRock Rack Instant Flash. Just launch this tool and save the new BIOS file to your USB flash drive, floppy disk or hard drive, then you can update your BIOS only in a few clicks without preparing an additional floppy diskette or other complicated flash utility. Please be noted that the USB flash drive or hard drive must use FAT32/16/12 file system.

1.4 Motherboard Layout



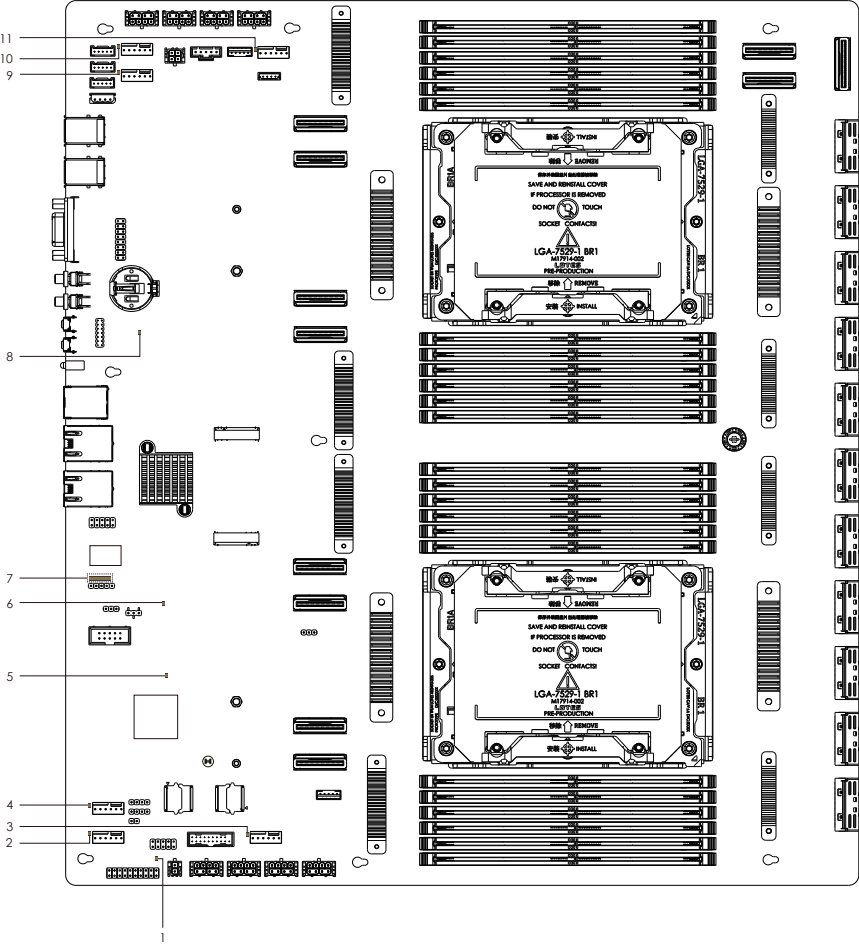
No.	Description
1	ATX 12V Power Connector (ATX12V1)
2	Micro-Fit Power Connector (ATX4PIN1)
3	ATX 12V Power Connector (ATX12V2)
4	PSU SMBus Header (PSU_SMB1)
5	ATX 12V Power Connector (ATX12V3)
6	Backplane PCI Express Hot-Plug Connector (CPU2_HSBP1)
7	ATX 12V Power Connector (ATX12V4)
8	System Fan Header (FAN3)
9	Virtual RAID On CPU Header (RAID_1)
10	Mini Cool Edge IO Connector (MCIO17)
11	Mini Cool Edge IO Connector (MCIO18)
12	3 DDR5 DIMM Slots (P2_DDR5_G1/I1/K1)*
13	3 DDR5 DIMM Slots (P2_DDR5_H1/J1/L1)*
14	Mini Cool Edge IO Connector (MCIO22)
15	Mini Cool Edge IO Connector (MCIO21)
16	Mini Cool Edge IO Connector (MCIO16)
17	Mini Cool Edge IO Connector (MCIO15)
18	Socket BR (LGA 7529) (CPU2)
19	Mini Cool Edge IO Connector (MCIO14)
20	3 DDR5 DIMM Slots (P2_DDR5_A1/C1/E1)*
21	Mini Cool Edge IO Connector (MCIO13)
22	3 DDR5 DIMM Slots (P2_DDR5_B1/D1/F1)*
23	Mini Cool Edge IO Connector (MCIO12)
24	Mini Cool Edge IO Connector (MCIO11)
25	Thumbscrew
26	Mini Cool Edge IO Connector (MCIO6)
27	3 DDR5 DIMM Slots (P1_DDR5_H1/J1/L1)*
28	Mini Cool Edge IO Connector (MCIO5)
29	3 DDR5 DIMM Slots (P1_DDR5_G1/I1/K1)*
30	Mini Cool Edge IO Connector (MCIO4)
31	Socket BR (LGA 7529) (CPU1)
32	Mini Cool Edge IO Connector (MCIO3)
33	Mini Cool Edge IO Connector (MCIO2)
34	Mini Cool Edge IO Connector (MCIO1)

No.	Description
35	3 DDR5 DIMM Slots (P1_DDR5_A1/C1/E1)*
36	3 DDR5 DIMM Slots (P1_DDR5_B1/D1/F1)*
37	Mini Cool Edge IO Connector (MCIO10)
38	Mini Cool Edge IO Connector (MCIO9)
39	Backplane PCI Express Hot-Plug Connector (CPU1_HSBP1)
40	ATX 12V Power Connector (ATX12V8)
41	ATX 12V Power Connector (ATX12V7)
42	System Fan Header (FAN4)
43	ATX 12V Power Connector (ATX12V6)
44	USB 3.2 Gen1 Header (USB3_1_2)
45	ATX 12V Power Connector (ATX12V5)
46	HDD Backplane Power Connector (BP_PWR1)
47	System Panel Header (PANEL1)
48	Auxiliary Panel Header (AUX_PANEL1)
49	IPMI LAN LED Header (IPMI_LED1)
50	System Fan Header (FAN6)
51	Non Maskable Interrupt Button (NMI_BTN1)
52	System Fan Header (FAN5)
53	Rear Panel LAN LED (RL_LED1)
54	Clear CMOS Pad (CLRMOS1)
55	Mini Cool Edge IO Connector (MCIO7)
56	PWM Configuration Header (PWM_CFG1)
57	COM Port Header (COM1)
58	M.2 Signal Source Selection Jumper (M2_NV_SEL1)
59	NCSI Mode Jumper (NCSI_SEL1)
60	Liquid Crystal Module Header (LCM1)
61	Mini Cool Edge IO Connector (MCIO8)
62	M.2 Socket (M2_1) (Type 2280/22110)
63	Network Controller Sideband Interface Header (NCSI1)
64	M.2 Socket (M2_2) (Type 2280/22110)
65	Mini Cool Edge IO Connector (MCIO19)
66	SPI TPM Header (TPM1)
67	Front VGA Header (FRNT_VGA1)
68	Mini Cool Edge IO Connector (MCIO20)

No.	Description
69	System Fan Header (FAN2)
70	Intelligent Platform Management Bus Header (IPMB1)
71	BMC SMBus Header (BMC_SMB3)
72	BMC SMBus Header (BMC_SMB2)
73	BMC SMBus Header (BMC_SMB1)
74	System Fan Header (FAN1)

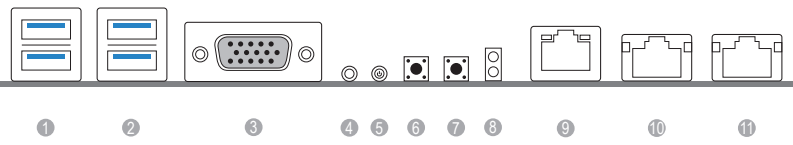
**For DIMM installation and configuration instructions, please see p.21 (Installing the Memory Modules (DIMM)) for more details.*

1.5 Onboard LED Indicators



No.	Item	Status	Description
1	SB_PWR1	Green	STB power ready
2	LED_FAN6	Red	FAN6 failed
3	LED_FAN4	Red	FAN4 failed
4	LED_FAN5	Red	FAN5 failed
5	BLED1	Blinking four times and then off	Start initialization after AC power-on or BMC reset
		Blinking at 1Hz	BMC ready
		Steady on	Error
		Steady off	(The actual behavior depends on the state at the time of failure)
		Other frequency	
6	LED_CPLD_HB1	Green	CPLD heartbeat LED
7	LED_POST1-8	Green	CPLD power-on status LED
8	LED_CATERR1	Red	System caterr LED
9	LED_FAN2	Red	FAN2 failed
10	LED_FAN1	Red	FAN1 failed
11	LED_FAN3	Red	FAN3 failed

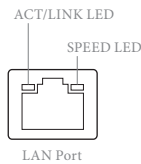
1.6 I/O Panel



No. Description		No. Description	
1	USB 3.2 Gen1 Ports (USB3_1_2)	7	NMI Button (NMI_BTN)
2	USB 3.2 Gen1 Ports (USB3_3_4)	8	HDD/System Fault LED (HDD_SYS_LED)
3	VGA Header (VGA1)	9	IPMI LAN Header (IPMI_LAN1)*
4	UID Switch/LED (UID1)	10	1G LAN RJ-45 Port (LAN1, shared NIC)**
5	Power Switch/LED (PWR_BTN)	11	1G LAN RJ-45 Port (LAN2)**
6	Reset Button (RST_BTN)		

LAN Port LED Indications

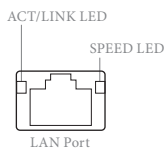
*There are two LEDs on the IPMI LAN port specified for link and speed. Please refer to the table below for the LAN port LED indications.



IPMI LAN Port LED Indications

Activity / Link LED		Speed LED	
Status	Description	Status	Description
Off	No link	Off	10 Mbps connection or no link
Blinking Yellow	Data activity	Orange	100 Mbps connection
On	Link	Green	1 Gbps connection

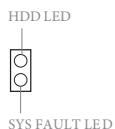
**There are two LEDs the 1G LAN port specified for link and speed. Please refer to the table below for the LAN port LED indications.



1G LAN Port (LAN1, LAN2) LED Indications

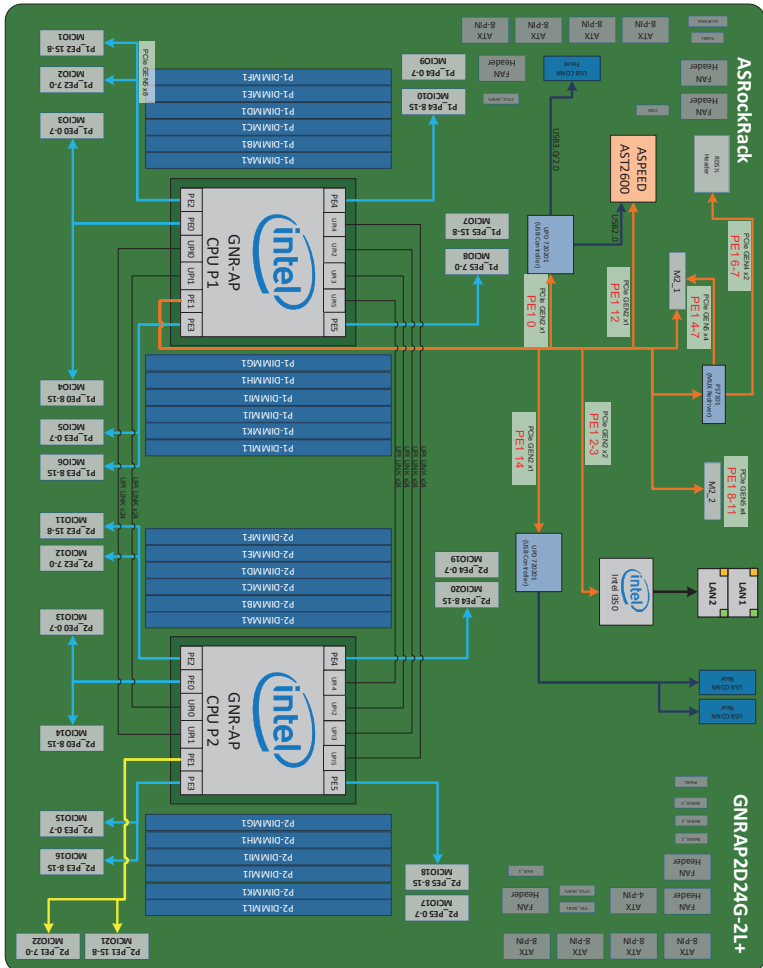
Activity / Link LED		Speed LED	
Status	Description	Status	Description
Off	No link	Off	100 M/10 Mbps connection or no link
Blinking Yellow	Data activity	Orange	100 Mbps connection
On	Link	Green	1 Gbps connection

HDD/System Fault LED Indications



HDD LED		SYS FAULT LED	
Status	Description	Status	Description
Off	HDD inactive	Off	Normal
Blinking Green	HDD active	Red	System failed

1.7 Block Diagram



Chapter 2 Installation

This is a proprietary form factor 16.93" x 15.17" (430 mm x 385.35 mm) motherboard. Before installing the motherboard, study the configuration of the chassis to ensure that the motherboard fits into it.



1. Ensure the motherboard battery is installed before unplugging the power cord or installing/removing the motherboard.
2. Before installing or removing any component, ensure that the power supply is off or the power cord is detached from the power supply. Failure to do so may cause severe damage to the motherboard, peripherals, and/or components.

2.1 Screw Holes

Place screws into the holes indicated by circles to secure the motherboard to the chassis.



Do not over-tighten the screws! Doing so may damage the motherboard.

2.2 Pre-installation Precautions

Take note of the following precautions before installing motherboard components or change any motherboard settings.

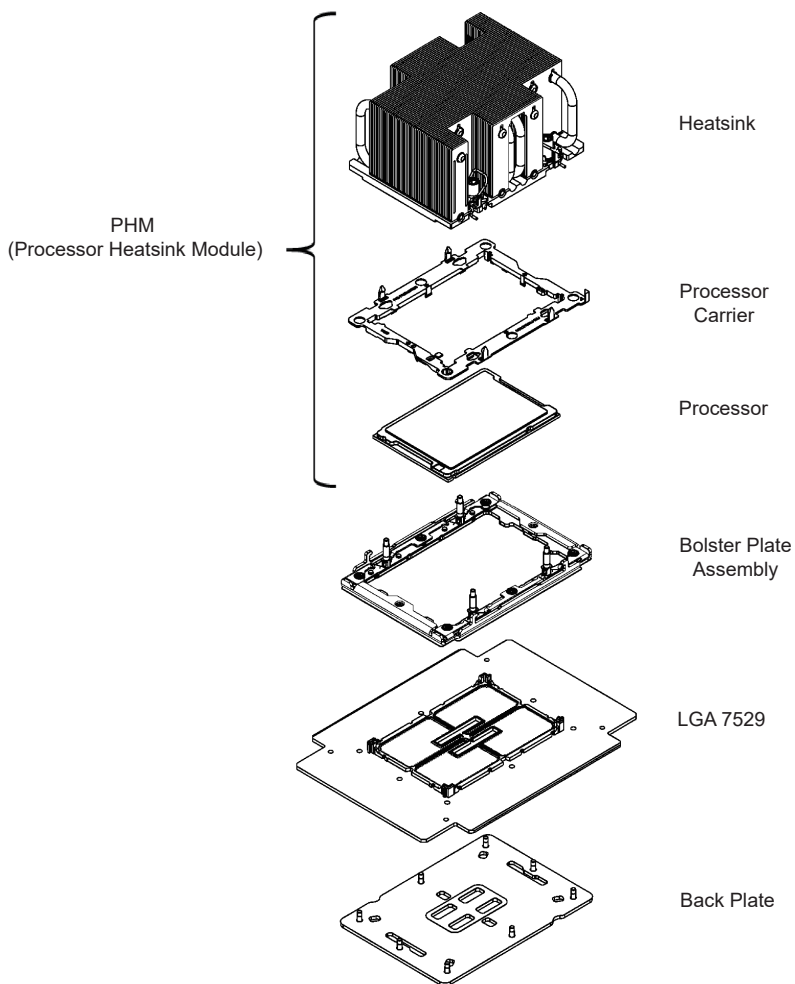
1. Unplug the power cord from the wall socket before touching any components.
2. To avoid damaging the motherboard's components due to static electricity, NEVER place the motherboard directly on the carpet or the like. Also remember to use a grounded wrist strap or touch a safety grounded object before handling the components.
3. Hold components by the edges and do not touch the ICs.
4. Whenever uninstall any component, place it on a grounded anti-static pad or in the bag that comes with the component.
5. When placing screws into the screw holes to secure the motherboard to the chassis, please do not over-tighten the screws! Doing so may damage the motherboard.

2.3 Installing the CPU and Heatsink



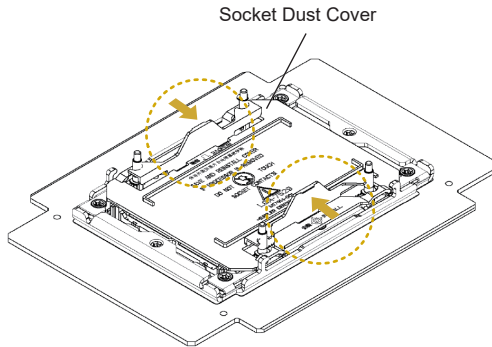
1. Unplug all power cables before installing the CPU.
2. Illustration in this documentation are examples only.

LGA7529 Enabling Components

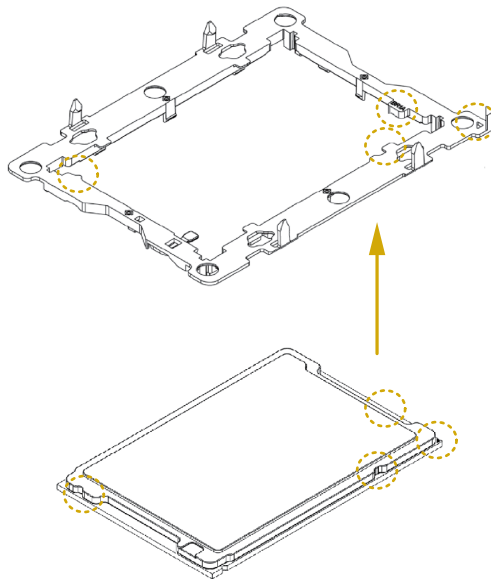


Follow the steps below to finish the CPU installation and please save the socket dust cover when returning for service.

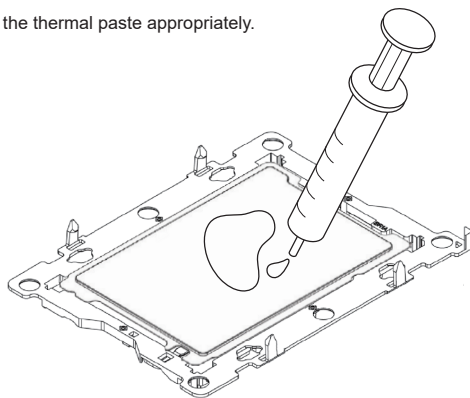
- 1 Removing the socket dust cover.



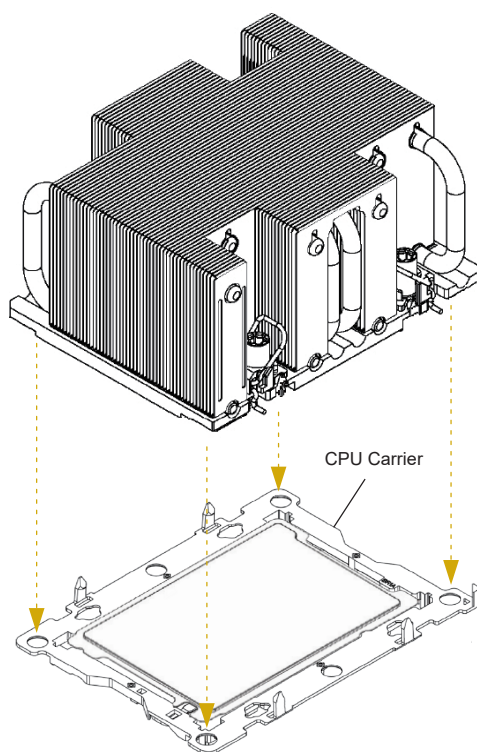
- 2 Installing the processor to the carrier and locking it in place.



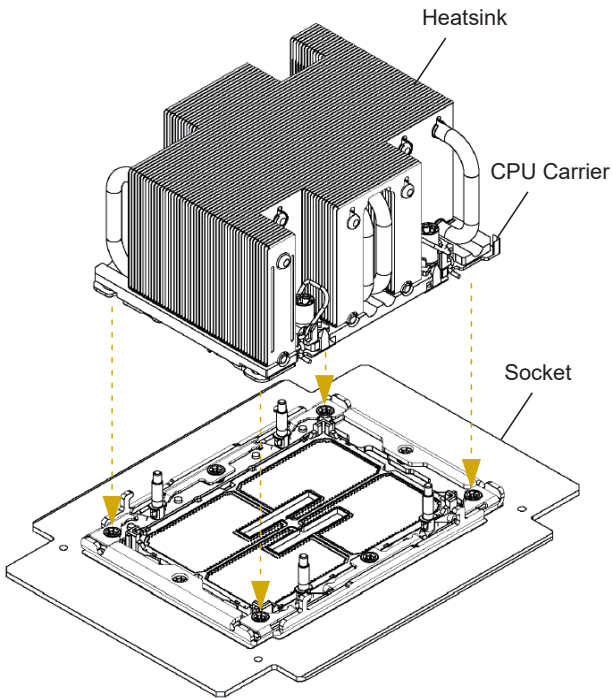
- 3 Applying the thermal paste appropriately.



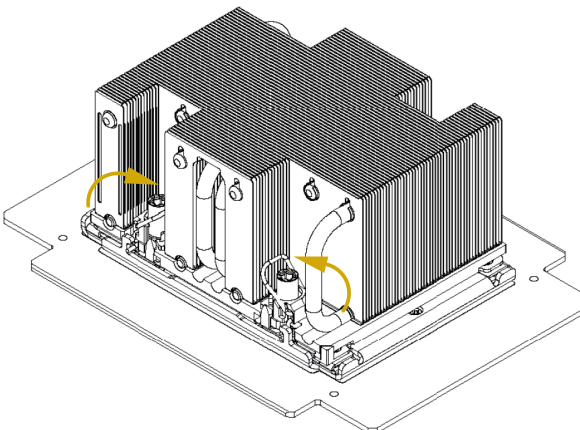
- 4 Installing the heatsink to CPU carrier.



5 Installing the PHM to the socket.



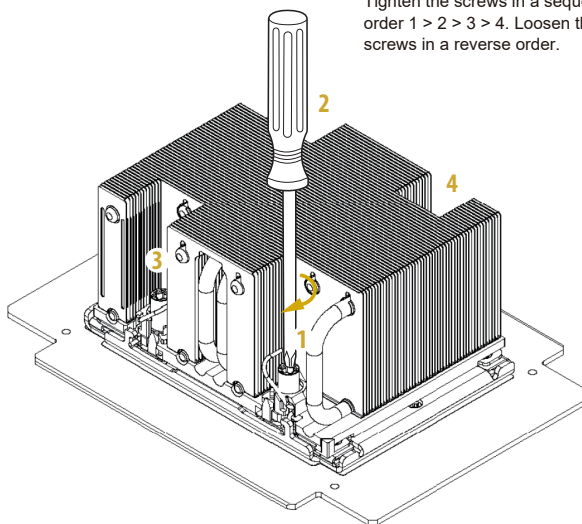
6 Latching the PHM.



7 Securing the screws.

Set the torque wrench to 6-12 in-lb.
One fourth a turn each time.

Tighten the screws in a sequential
order 1 > 2 > 3 > 4. Loosen the
screws in a reverse order.



2.4 Installing the Memory Modules (DIMM)

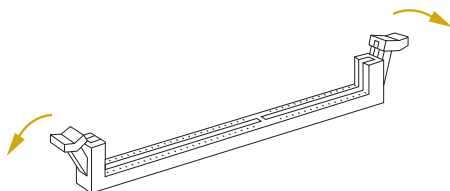
This motherboard provides twenty-four 288-pin DDR5 (Double Data Rate 5) DIMM slots in two groups, and supports Single Channel Memory Technology.

CPU1	CPU2
P1_DDR5_A1, B1, C1, D1, E1, F1	P2_DDR5_A1, B1, C1, D1, E1, F1
P1_DDR5_G1, H1, I1, J1, K1, L1	P2_DDR5_G1, H1, I1, J1, K1, L1

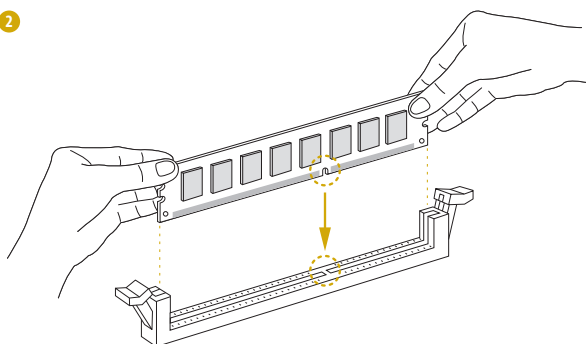


1. It is not allowed to install a DDR, DDR2, DDR3 or DDR4 memory module into a DDR5 slot; otherwise, this motherboard and DIMM may be damaged.
2. For Single channel configuration, it always needs to install identical (the same brand, speed, size and chip-type) DDR5 DIMMs.

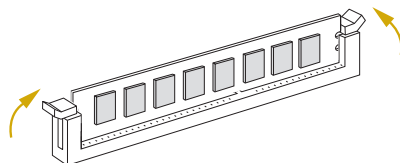
1



2



3

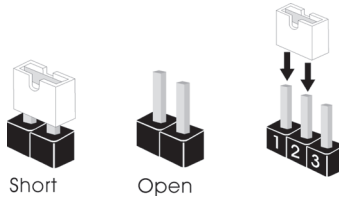


Recommended Memory Configurations

Number of Memory Channels Populated	Number of CPU Installed	Recommended Memory Channels																							
		CPU1												CPU2											
		A1	B1	C1	D1	E1	F1	G1	H1	I1	J1	K1	L1	A1	B1	C1	D1	E1	F1	G1	H1	I1	J1	K1	L1
24	2P	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	1P																								
16	2P			V	V	V	V			V	V	V	V			V	V	V	V			V	V	V	V
	1P																								
12	2P																								
	1P	V	V	V	V	V	V	V	V	V	V	V	V												
8	2P																								
	1P			V	V	V	V			V	V	V	V												
2	2P	V											V												
	1P																								
1	2P																								
	1P	V																							

2.5 Jumper Setup

The illustration shows how jumpers are setup. When the jumper cap is placed on the pins, the jumper is “Short”. If no jumper cap is placed on the pins, the jumper is “Open”. The illustration shows a 3-pin jumper whose pin1 and pin2 are “Short” when a jumper cap is placed on these 2 pins.



M.2 Signal Source

Selection Jumper

(3-pin M2_NV_SEL1)

(see p.6, No. 58)



M.2_1 (x4) (Default)



RDS (x2) + M.2_1 (x2)

NCSI Mode Jumper

(3-pin NCSI_SEL1)

(see p.6, No. 59)



NCSI to I350 (Default)



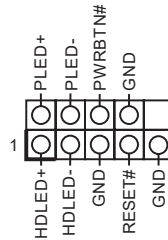
Share to NCSI Header

2.6 Onboard Headers and Connectors



Onboard headers and connectors are NOT jumpers. Do NOT place jumper caps over these headers and connectors. Placing jumper caps over the headers and connectors will cause permanent damage to the motherboard.

System Panel Header
(9-pin PANEL1)
(see p.6, No.47)



Connect the power switch, reset switch and system status indicator on the chassis to this header according to the pin assignments. Particularly note the positive and negative pins before connecting the cables.



PWRBTN (Power Switch):

Connect to the power switch on the chassis front panel and configure the way to turn off the system using the power switch.

RESET (Reset Switch):

Connect to the reset switch on the chassis front panel. Press the reset switch to restart the computer if the computer freezes and fails to perform a normal restart.

PLED (System Power LED):

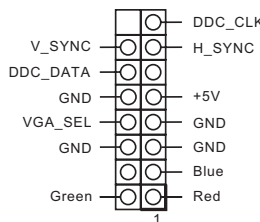
Connect to the power status indicator on the chassis front panel. The LED is on when the system is operating. The LED is off when the system is in S4 sleep state or powered off (S5).

HDLED (Hard Drive Activity LED):

Connect to the hard drive activity LED on the chassis front panel. The LED is on when the hard drive is reading or writing data.

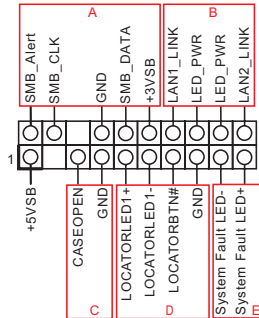
The front panel design may differ by chassis. A front panel module mainly consists of power switch, reset switch, power LED, hard drive activity LED, speaker and etc. When connecting the chassis front panel module to this header, make sure the wire assignments and the pin assignments are matched correctly.

Front VGA Header
(15-pin FRNT_VGA1)
(see p.6, No. 67)



Please connect either end of VGA cable to VGA header.

Auxiliary Panel Header
(18-pin AUX PANEL1)
(see p.6, No.48)



This header supports multiple functions on the front panel, including the front panel SMB, internet status indicator and chassis intrusion pin.



A. Front panel SMBus connecting pin (6-1 pin FPSMB):

This header allows user to connect SMBus (System Management Bus) equipment. It can be used for communication between peripheral equipment in the system, which has slower transmission rates, and power management equipment.

B. Internet status indicator (4-pin LAN, LED):

This header allows user to use the Gigabit internet indicator cable to connect to the LAN status indicator. When this indicator flickers, it means that the internet is properly connected.

C. Chassis intrusion pin (2-pin CHASSIS):

This header is provided for host computer chassis with chassis intrusion detection designs. In addition, it must also work with external detection equipment, such as a chassis intrusion detection sensor or a microswitch. When this function is activated, if any chassis component movement occurs, the sensor will immediately detect it and send a signal to this header, and the system will then record this chassis intrusion event. The default setting is set to the CASEOPEN and GND pin; this function is off.

D. Locator LED (4-pin LOCATOR):

This header is for the locator switch and LED on the front panel.

E. System Fault LED (2-pin SYSTEM STATUS):

This header is for the Fault LED on the system.

Non Maskable Interrupt
Button Header
(NMI_BTN1)
(see p.6, No.51)



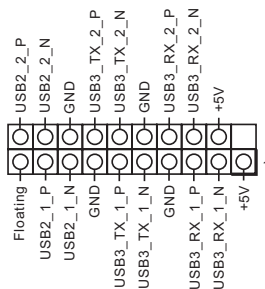
Please connect a NMI device to this header.

PWM Configuration
Header
(3-pin PWM_CFG1)
(see p.6, No.56)



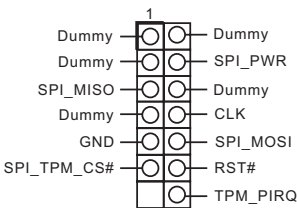
This header is used for PWM configurations.

USB 3.2 Gen1 Header
(19-pin USB3_1_2)
(see p.6, No.44)



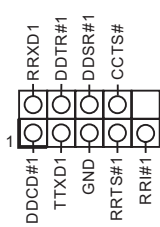
Besides two default USB 3.2 Gen1 ports on the I/O panel, there is one USB 3.2 Gen1 header on this motherboard. This USB 3.2 Gen1 header can support two USB 3.2 Gen1 ports.

SPI TPM Header
(13-pin TPM1)
(see p.6, No.66)



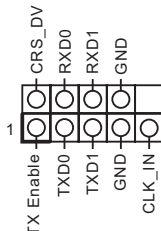
This connector supports SPI Trusted Platform Module (TPM) system, which can securely store keys, digital certificates, passwords, and data. A TPM system also helps enhance network security, protects digital identities, and ensures platform integrity.

COM Port Header
(9-pin COM1)
(see p.6, No.57)



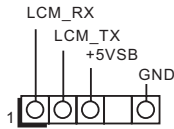
This COM1 header supports a serial port module.

Network Controller Side-band Interface Header
(9-pin NCSI)
(see p.6, No.63)



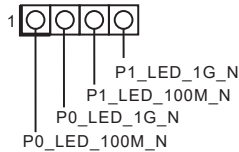
The onboard NCSI header is used for external connections..

Liquid Crystal Module
Header
(4-pin LCM1)
(see p.6, No. 60)



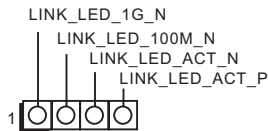
This header is used for extended Liquid Crystal Module (LCM) on the front panel of a server system.

Rear Panel LAN LED
(4-pin RL_LED1)
(see p.6, No. 53)



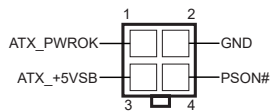
This header is used for extended LAN LED on the rear panel of a server system.

IPMI LAN LED Header
(4-pin IPMI_LED1)
(see p.6, No. 49)



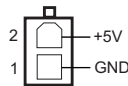
This header is used to connect to the LED indicators on the chassis.

Micro-Fit Power
Connector
(4-pin ATX4PIN1)
(see p.6, No. 2)



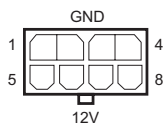
The motherboard provides one 4-pin power/signal connector which is a required input for ATX power source. When using ATX power, it is necessary to use a 24pin to 4pin power cable to connect between the 24pin power connector of PSU and the ATX4PIN1 connector on the motherboard for power supply and signal communication.

HDD Backplane Power
Connector
(2-pin BP_PWR1)
(see p.6, No. 46)



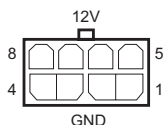
Please connect a 2-pin power cable to this connector to connect a HDD.

ATX 12V Power
Connectors
(8-pin ATX12V1)
(see p.6, No.1)
(8-pin ATX12V2)
(see p.6, No.3)
(8-pin ATX12V3)
(see p.6, No.5)
(8-pin ATX12V4)
(see p.6, No.7)

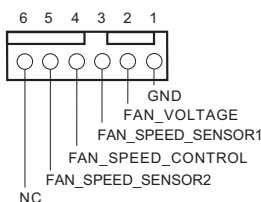


This motherboard provides
eight Micro-Hi 8-pin ATX
12V power connectors.

(8-pin ATX12V5)
(see p.6, No.45)
(8-pin ATX12V6)
(see p.6, No.43)
(8-pin ATX12V7)
(see p.6, No.41)
(8-pin ATX12V8)
(see p.6, No.40)

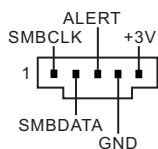


System Fan Headers
(6-pin FAN1)
(see p.6, No.74)
(6-pin FAN2)
(see p.6, No.69)
(6-pin FAN3)
(see p.6, No.8)
(6-pin FAN4)
(see p.6, No.42)
(6-pin FAN5)
(see p.6, No.52)
(6-pin FAN6)
(see p.6, No.50)



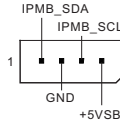
Please connect fan cables to
the fan connectors and match
the black wire to the ground
pin. All fans support Fan
Control. The fan max. current
is 5A and the max. power is
60 Watts.

PSU SMBus Header
(PSU_SMB1)
(see p.6, No.4)



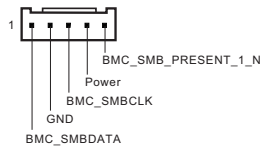
PSU SMBus monitors the
status of the power supply, fan
and system temperature.

Intelligent Platform
Management Bus header
(4-pin IPMB1)
(see p.6, No.70)



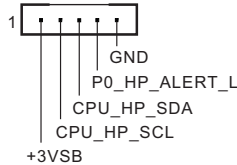
This 4-pin connector is used to provide a cabled base-board or front panel connection for value added features and 3rd-party add-in cards, such as Emergency Management cards, that provide management features using the IPMB.

BMC SMBus Headers
(5-pin BMC_SMB1)
(see p.6, No.73)
(5-pin BMC_SMB2)
(see p.6, No.72)
(5-pin BMC_SMB3)
(see p.6, No.71)



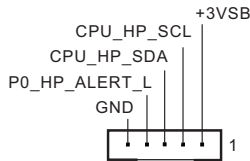
These headers are used for the SM BUS devices.

Backplane PCI Express
Hot-Plug Connectors
(5-pin CPU1_HSBP1)
(see p.6, No.39)



This header is used for the hot plug feature of HDDs on the backplane.

(5-pin CPU2_HSBP1)
(see p.6, No.6)

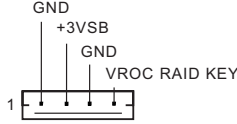


Clear CMOS Pad
(CLRMOS1)
(see p.6, No.54)



CLRMOS1 allows user to clear the data in CMOS. To clear CMOS, take out the CMOS battery and short the Clear CMOS Pad.

Virtual RAID On CPU
Header
(4-pin RAID_1)
(see p.6, No.9)



This connector supports Intel®
Virtual RAID on CPU and
NVME/AHCI RAID on CPU
PCIE.

With the introduction of the Intel VROC product, there are three modes of operation:

SKU	HW key required	Key features
Pass-thru	Not needed	• Pass-thru only (no RAID) • LED Management • Hot Plug Support • RAID 0 support for Intel Fultondale NVMe SSDs
Standard	VROCSTANMOD	• Pass-thru SKU features • RAID 0, 1, 10
Premium	VROCPREMMOD	• Standard SKU features • RAID 5
ISS	VROCISSDMOD	• RAID 5 Write Hole Closure

*Only Intel SSDs are supported.
*For further details on VROC, please refer to the official information released by Intel.

Mini Cool Edge IO
Connectors

Right-Angle:

(MCIO1)

(see p.6, No.34)

(MCIO2)

(see p.6, No.33)

(MCIO3)

(see p.6, No.32)

(MCIO4)

(see p.6, No.30)

(MCIO5)

(see p.6, No.28)

(MCIO6)

(see p.6, No.26)

(MCIO11)

(see p.6, No.24)

(MCIO12)

(see p.6, No.23)

(MCIO13)

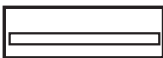
(see p.6, No.21)

(MCIO14)

(see p.6, No.19)

(MCIO15)

(see p.6, No.17)



These connectors are used for
the PCIe devices.

**Up to 4 CXL devices supported per
socket; CXL memory function only
supported at PCIe x16 bifurcation*

Mini Cool Edge IO
Connectors

Vertical:

(MCIO7)

(see p.6, No.55)

(MCIO8)

(see p.6, No.61)

(MCIO9)

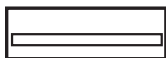
(see p.6, No.38)

(MCIO10)

(see p.6, No.37)

(MCIO16)

(see p.6, No.16)



These connectors are used for
the PCIE devices.

**Up to 4 CXL devices supported per
socket; CXL memory function only
supported at PCIe x16 bifurcation*



(MCIO17)

(see p.6, No.10)

(MCIO18)

(see p.6, No.11)

(MCIO19)

(see p.6, No.65)

(MCIO20)

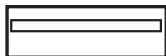
(see p.6, No.68)

(MCIO21)

(see p.6, No.15)

(MCIO22)

(see p.6, No.14)



MCIO1 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE2_RX_DP15	B2	PE2_TX_DP15
A3	PE2_RX_DN15	B3	PE2_TX_DN15
A4	GND	B4	GND
A5	PE2_RX_DN14	B5	PE2_TX_DN14
A6	PE2_RX_DP14	B6	PE2_TX_DP14
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSTNT1
A13	GND	B13	GND
A14	PE2_RX_DP13	B14	PE2_TX_DP13
A15	PE2_RX_DN13	B15	PE2_TX_DN13
A16	GND	B16	GND
A17	PE2_RX_DP12	B17	PE2_TX_DN12
A18	PE2_RX_DN12	B18	PE2_TX_DP12
A19	GND	B19	GND
A20	PE2_RX_DN11	B20	PE2_TX_DP11
A21	PE2_RX_DP11	B21	PE2_TX_DN11
A22	GND	B22	GND
A23	PE2_RX_DN10	B23	PE2_TX_DN10
A24	PE2_RX_DP10	B24	PE2_TX_DP10
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSTNT2
A31	GND	B31	GND
A32	PE2_RX_DN9	B32	PE2_TX_DP9
A33	PE2_RX_DP9	B33	PE2_TX_DN9
A34	GND	B34	GND
A35	PE2_RX_DN8	B35	PE2_TX_DN8
A36	PE2_RX_DP8	B36	PE2_TX_DP8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO2 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE2_RX_DP7	B2	PE2_TX_DP7
A3	PE2_RX_DN7	B3	PE2_TX_DN7
A4	GND	B4	GND
A5	PE2_RX_DP6	B5	PE2_TX_DN6
A6	PE2_RX_DN6	B6	PE2_TX_DP6
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSNT1
A13	GND	B13	GND
A14	PE2_RX_DP5	B14	PE2_TX_DP5
A15	PE2_RX_DN5	B15	PE2_TX_DN5
A16	GND	B16	GND
A17	PE2_RX_DP4	B17	PE2_TX_DN4
A18	PE2_RX_DN4	B18	PE2_TX_DP4
A19	GND	B19	GND
A20	PE2_RX_DN3	B20	PE2_TX_DP3
A21	PE2_RX_DP3	B21	PE2_TX_DN3
A22	GND	B22	GND
A23	PE2_RX_DN2	B23	PE2_TX_DN2
A24	PE2_RX_DP2	B24	PE2_TX_DP2
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSNT2
A31	GND	B31	GND
A32	PE2_RX_DN1	B32	PE2_TX_DP1
A33	PE2_RX_DP1	B33	PE2_TX_DN1
A34	GND	B34	GND
A35	PE2_RX_DN0	B35	PE2_TX_DN0
A36	PE2_RX_DP0	B36	PE2_TX_DP0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO3 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE0_RX_DP0	B2	PE0_TX_DP0
A3	PE0_RX_DN0	B3	PE0_TX_DN0
A4	GND	B4	GND
A5	PE0_RX_DP1	B5	PE0_TX_DN1
A6	PE0_RX_DN1	B6	PE0_TX_DP1
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSTNT1
A13	GND	B13	GND
A14	PE0_RX_DP2	B14	PE0_TX_DN2
A15	PE0_RX_DN2	B15	PE0_TX_DP2
A16	GND	B16	GND
A17	PE0_RX_DP3	B17	PE0_TX_DN3
A18	PE0_RX_DN3	B18	PE0_TX_DP3
A19	GND	B19	GND
A20	PE0_RX_DP4	B20	PE0_TX_DP4
A21	PE0_RX_DN4	B21	PE0_TX_DN4
A22	GND	B22	GND
A23	PE0_RX_DP5	B23	PE0_TX_DP5
A24	PE0_RX_DN5	B24	PE0_TX_DN5
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSTNT2
A31	GND	B31	GND
A32	PE0_RX_DP6	B32	PE0_TX_DP6
A33	PE0_RX_DN6	B33	PE0_TX_DN6
A34	GND	B34	GND
A35	PE0_RX_DP7	B35	PE0_TX_DP7
A36	PE0_RX_DN7	B36	PE0_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO4 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE0_RX_DP8	B2	PE0_TX_DP8
A3	PE0_RX_DN8	B3	PE0_TX_DN8
A4	GND	B4	GND
A5	PE0_RX_DP9	B5	PE0_TX_DP9
A6	PE0_RX_DN9	B6	PE0_TX_DN9
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSNT1
A13	GND	B13	GND
A14	PE0_RX_DP10	B14	PE0_TX_DP10
A15	PE0_RX_DN10	B15	PE0_TX_DN10
A16	GND	B16	GND
A17	PE0_RX_DP11	B17	PE0_TX_DP11
A18	PE0_RX_DN11	B18	PE0_TX_DN11
A19	GND	B19	GND
A20	PE0_RX_DN12	B20	PE0_TX_DP12
A21	PE0_RX_DP12	B21	PE0_TX_DN12
A22	GND	B22	GND
A23	PE0_RX_DN13	B23	PE0_TX_DN13
A24	PE0_RX_DP13	B24	PE0_TX_DP13
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSNT2
A31	GND	B31	GND
A32	PE0_RX_DN14	B32	PE0_TX_DP14
A33	PE0_RX_DP14	B33	PE0_TX_DN14
A34	GND	B34	GND
A35	PE0_RX_DP15	B35	PE0_TX_DP15
A36	PE0_RX_DN15	B36	PE0_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO5 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE3_RX_DP0	B2	PE3_TX_DP0
A3	PE3_RX_DN0	B3	PE3_TX_DN0
A4	GND	B4	GND
A5	PE3_RX_DN1	B5	PE3_TX_DN1
A6	PE3_RX_DP1	B6	PE3_TX_DP1
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSENT1
A13	GND	B13	GND
A14	PE3_RX_DP2	B14	PE3_TX_DP2
A15	PE3_RX_DN2	B15	PE3_TX_DN2
A16	GND	B16	GND
A17	PE3_RX_DN3	B17	PE3_TX_DN3
A18	PE3_RX_DP3	B18	PE3_TX_DP3
A19	GND	B19	GND
A20	PE3_RX_DP4	B20	PE3_TX_DP4
A21	PE3_RX_DN4	B21	PE3_TX_DN4
A22	GND	B22	GND
A23	PE3_RX_DN5	B23	PE3_TX_DN5
A24	PE3_RX_DP5	B24	PE3_TX_DP5
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSENT2
A31	GND	B31	GND
A32	PE3_RX_DP6	B32	PE3_TX_DP6
A33	PE3_RX_DN6	B33	PE3_TX_DN6
A34	GND	B34	GND
A35	PE3_RX_DN7	B35	PE3_TX_DN7
A36	PE3_RX_DP7	B36	PE3_TX_DP7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO6 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE3_RX_DP8	B2	PE3_TX_DP8
A3	PE3_RX_DN8	B3	PE3_TX_DN8
A4	GND	B4	GND
A5	PE3_RX_DN9	B5	PE3_TX_DN9
A6	PE3_RX_DP9	B6	PE3_TX_DP9
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSNT1
A13	GND	B13	GND
A14	PE3_RX_DP10	B14	PE3_TX_DP10
A15	PE3_RX_DN10	B15	PE3_TX_DN10
A16	GND	B16	GND
A17	PE3_RX_DN11	B17	PE3_TX_DN11
A18	PE3_RX_DP11	B18	PE3_TX_DP11
A19	GND	B19	GND
A20	PE3_RX_DP12	B20	PE3_TX_DP12
A21	PE3_RX_DN12	B21	PE3_TX_DN12
A22	GND	B22	GND
A23	PE3_RX_DN13	B23	PE3_TX_DN13
A24	PE3_RX_DP13	B24	PE3_TX_DP13
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSNT2
A31	GND	B31	GND
A32	PE3_RX_DP14	B32	PE3_TX_DP14
A33	PE3_RX_DN14	B33	PE3_TX_DN14
A34	GND	B34	GND
A35	PE3_RX_DN15	B35	PE3_TX_DN15
A36	PE3_RX_DP15	B36	PE3_TX_DP15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO7 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE5_RX_DP15	B2	PE5_TX_DP15
A3	PE5_RX_DN15	B3	PE5_TX_DN15
A4	GND	B4	GND
A5	PE5_RX_DP14	B5	PE5_TX_DP14
A6	PE5_RX_DN14	B6	PE5_TX_DN14
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSENT1
A13	GND	B13	GND
A14	PE5_RX_DP13	B14	PE5_TX_DP13
A15	PE5_RX_DN13	B15	PE5_TX_DN13
A16	GND	B16	GND
A17	PE5_RX_DP12	B17	PE5_TX_DN12
A18	PE5_RX_DN12	B18	PE5_TX_DP12
A19	GND	B19	GND
A20	PE5_RX_DP11	B20	PE5_TX_DP11
A21	PE5_RX_DN11	B21	PE5_TX_DN11
A22	GND	B22	GND
A23	PE5_RX_DP10	B23	PE5_TX_DP10
A24	PE5_RX_DN10	B24	PE5_TX_DN10
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSENT2
A31	GND	B31	GND
A32	PE5_RX_DP9	B32	PE5_TX_DP9
A33	PE5_RX_DN9	B33	PE5_TX_DN9
A34	GND	B34	GND
A35	PE5_RX_DP8	B35	PE5_TX_DP8
A36	PE5_RX_DN8	B36	PE5_TX_DN8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO8 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE5_RX_DP7	B2	PE5_TX_DP7
A3	PE5_RX_DN7	B3	PE5_TX_DN7
A4	GND	B4	GND
A5	PE5_RX_DP6	B5	PE5_TX_DP6
A6	PE5_RX_DN6	B6	PE5_TX_DN6
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSNT1
A13	GND	B13	GND
A14	PE5_RX_DP5	B14	PE5_TX_DP5
A15	PE5_RX_DN5	B15	PE5_TX_DN5
A16	GND	B16	GND
A17	PE5_RX_DP4	B17	PE5_TX_DN4
A18	PE5_RX_DN4	B18	PE5_TX_DP4
A19	GND	B19	GND
A20	PE5_RX_DP3	B20	PE5_TX_DN3
A21	PE5_RX_DN3	B21	PE5_TX_DP3
A22	GND	B22	GND
A23	PE5_RX_DP2	B23	PE5_TX_DN2
A24	PE5_RX_DN2	B24	PE5_TX_DP2
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSNT2
A31	GND	B31	GND
A32	PE5_RX_DP1	B32	PE5_TX_DP1
A33	PE5_RX_DN1	B33	PE5_TX_DN1
A34	GND	B34	GND
A35	PE5_RX_DP0	B35	PE5_TX_DP0
A36	PE5_RX_DN0	B36	PE5_TX_DN0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO9 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE4_RX_DN0	B2	PE4_TX_DP0
A3	PE4_RX_DP0	B3	PE4_TX_DN0
A4	GND	B4	GND
A5	PE4_RX_DN1	B5	PE4_TX_DP1
A6	PE4_RX_DP1	B6	PE4_TX_DN1
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSN1
A13	GND	B13	GND
A14	PE4_RX_DP2	B14	PE4_TX_DP2
A15	PE4_RX_DN2	B15	PE4_TX_DN2
A16	GND	B16	GND
A17	PE4_RX_DP3	B17	PE4_TX_DP3
A18	PE4_RX_DN3	B18	PE4_TX_DN3
A19	GND	B19	GND
A20	PE4_RX_DN4	B20	PE4_TX_DP4
A21	PE4_RX_DP4	B21	PE4_TX_DN4
A22	GND	B22	GND
A23	PE4_RX_DP5	B23	PE4_TX_DP5
A24	PE4_RX_DN5	B24	PE4_TX_DN5
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSN2
A31	GND	B31	GND
A32	PE4_RX_DP6	B32	PE4_TX_DP6
A33	PE4_RX_DN6	B33	PE4_TX_DN6
A34	GND	B34	GND
A35	PE4_RX_DP7	B35	PE4_TX_DN7
A36	PE4_RX_DN7	B36	PE4_TX_DP7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO10 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE4_RX_DP8	B2	PE4_TX_DP8
A3	PE4_RX_DN8	B3	PE4_TX_DN8
A4	GND	B4	GND
A5	PE4_RX_DP9	B5	PE4_TX_DP9
A6	PE4_RX_DN9	B6	PE4_TX_DN9
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSNT1
A13	GND	B13	GND
A14	PE4_RX_DP10	B14	PE4_TX_DP10
A15	PE4_RX_DN10	B15	PE4_TX_DN10
A16	GND	B16	GND
A17	PE4_RX_DP11	B17	PE4_TX_DP11
A18	PE4_RX_DN11	B18	PE4_TX_DN11
A19	GND	B19	GND
A20	PE4_RX_DN12	B20	PE4_TX_DP12
A21	PE4_RX_DP12	B21	PE4_TX_DN12
A22	GND	B22	GND
A23	PE4_RX_DN13	B23	PE4_TX_DP13
A24	PE4_RX_DP13	B24	PE4_TX_DN13
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSNT2
A31	GND	B31	GND
A32	PE4_RX_DN14	B32	PE4_TX_DP14
A33	PE4_RX_DP14	B33	PE4_TX_DN14
A34	GND	B34	GND
A35	PE4_RX_DP15	B35	PE4_TX_DP15
A36	PE4_RX_DN15	B36	PE4_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO11 Pin Definition [CPU2]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE2_RX_DP15	B2	PE2_TX_DP15
A3	PE2_RX_DN15	B3	PE2_TX_DN15
A4	GND	B4	GND
A5	PE2_RX_DN14	B5	PE2_TX_DN14
A6	PE2_RX_DP14	B6	PE2_TX_DP14
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSTNT1
A13	GND	B13	GND
A14	PE2_RX_DP13	B14	PE2_TX_DP13
A15	PE2_RX_DN13	B15	PE2_TX_DN13
A16	GND	B16	GND
A17	PE2_RX_DP12	B17	PE2_TX_DN12
A18	PE2_RX_DN12	B18	PE2_TX_DP12
A19	GND	B19	GND
A20	PE2_RX_DN11	B20	PE2_TX_DP11
A21	PE2_RX_DP11	B21	PE2_TX_DN11
A22	GND	B22	GND
A23	PE2_RX_DN10	B23	PE2_TX_DN10
A24	PE2_RX_DP10	B24	PE2_TX_DP10
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSTNT2
A31	GND	B31	GND
A32	PE2_RX_DN9	B32	PE2_TX_DP9
A33	PE2_RX_DP9	B33	PE2_TX_DN9
A34	GND	B34	GND
A35	PE2_RX_DN8	B35	PE2_TX_DN8
A36	PE2_RX_DP8	B36	PE2_TX_DP8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO12 Pin Definition [CPU2]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE2_RX_DP7	B2	PE2_TX_DP7
A3	PE2_RX_DN7	B3	PE2_TX_DN7
A4	GND	B4	GND
A5	PE2_RX_DP6	B5	PE2_TX_DN6
A6	PE2_RX_DN6	B6	PE2_TX_DP6
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSNT1
A13	GND	B13	GND
A14	PE2_RX_DP5	B14	PE2_TX_DP5
A15	PE2_RX_DN5	B15	PE2_TX_DN5
A16	GND	B16	GND
A17	PE2_RX_DP4	B17	PE2_TX_DN4
A18	PE2_RX_DN4	B18	PE2_TX_DP4
A19	GND	B19	GND
A20	PE2_RX_DN3	B20	PE2_TX_DP3
A21	PE2_RX_DP3	B21	PE2_TX_DN3
A22	GND	B22	GND
A23	PE2_RX_DN2	B23	PE2_TX_DN2
A24	PE2_RX_DP2	B24	PE2_TX_DP2
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSNT2
A31	GND	B31	GND
A32	PE2_RX_DN1	B32	PE2_TX_DP1
A33	PE2_RX_DP1	B33	PE2_TX_DN1
A34	GND	B34	GND
A35	PE2_RX_DN0	B35	PE2_TX_DN0
A36	PE2_RX_DP0	B36	PE2_TX_DP0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO13 Pin Definition [CPU2]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE0_RX_DP0	B2	PE0_TX_DP0
A3	PE0_RX_DN0	B3	PE0_TX_DN0
A4	GND	B4	GND
A5	PE0_RX_DP1	B5	PE0_TX_DN1
A6	PE0_RX_DN1	B6	PE0_TX_DP1
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSN1
A13	GND	B13	GND
A14	PE0_RX_DP2	B14	PE0_TX_DN2
A15	PE0_RX_DN2	B15	PE0_TX_DP2
A16	GND	B16	GND
A17	PE0_RX_DP3	B17	PE0_TX_DN3
A18	PE0_RX_DN3	B18	PE0_TX_DP3
A19	GND	B19	GND
A20	PE0_RX_DP4	B20	PE0_TX_DP4
A21	PE0_RX_DN4	B21	PE0_TX_DN4
A22	GND	B22	GND
A23	PE0_RX_DP5	B23	PE0_TX_DP5
A24	PE0_RX_DN5	B24	PE0_TX_DN5
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSN2
A31	GND	B31	GND
A32	PE0_RX_DP6	B32	PE0_TX_DP6
A33	PE0_RX_DN6	B33	PE0_TX_DN6
A34	GND	B34	GND
A35	PE0_RX_DP7	B35	PE0_TX_DP7
A36	PE0_RX_DN7	B36	PE0_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO14 Pin Definition [CPU2]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE0_RX_DP8	B2	PE0_TX_DP8
A3	PE0_RX_DN8	B3	PE0_TX_DN8
A4	GND	B4	GND
A5	PE0_RX_DP9	B5	PE0_TX_DP9
A6	PE0_RX_DN9	B6	PE0_TX_DN9
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSNT1
A13	GND	B13	GND
A14	PE0_RX_DP10	B14	PE0_TX_DP10
A15	PE0_RX_DN10	B15	PE0_TX_DN10
A16	GND	B16	GND
A17	PE0_RX_DP11	B17	PE0_TX_DP11
A18	PE0_RX_DN11	B18	PE0_TX_DN11
A19	GND	B19	GND
A20	PE0_RX_DN12	B20	PE0_TX_DP12
A21	PE0_RX_DP12	B21	PE0_TX_DN12
A22	GND	B22	GND
A23	PE0_RX_DN13	B23	PE0_TX_DN13
A24	PE0_RX_DP13	B24	PE0_TX_DP13
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSNT2
A31	GND	B31	GND
A32	PE0_RX_DN14	B32	PE0_TX_DP14
A33	PE0_RX_DP14	B33	PE0_TX_DN14
A34	GND	B34	GND
A35	PE0_RX_DP15	B35	PE0_TX_DP15
A36	PE0_RX_DN15	B36	PE0_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO15 Pin Definition [CPU2]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE3_RX_DP0	B2	PE3_TX_DP0
A3	PE3_RX_DN0	B3	PE3_TX_DN0
A4	GND	B4	GND
A5	PE3_RX_DN1	B5	PE3_TX_DN1
A6	PE3_RX_DP1	B6	PE3_TX_DP1
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSENT1
A13	GND	B13	GND
A14	PE3_RX_DP2	B14	PE3_TX_DP2
A15	PE3_RX_DN2	B15	PE3_TX_DN2
A16	GND	B16	GND
A17	PE3_RX_DN3	B17	PE3_TX_DN3
A18	PE3_RX_DP3	B18	PE3_TX_DP3
A19	GND	B19	GND
A20	PE3_RX_DP4	B20	PE3_TX_DP4
A21	PE3_RX_DN4	B21	PE3_TX_DN4
A22	GND	B22	GND
A23	PE3_RX_DN5	B23	PE3_TX_DN5
A24	PE3_RX_DP5	B24	PE3_TX_DP5
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSENT2
A31	GND	B31	GND
A32	PE3_RX_DP6	B32	PE3_TX_DP6
A33	PE3_RX_DN6	B33	PE3_TX_DN6
A34	GND	B34	GND
A35	PE3_RX_DN7	B35	PE3_TX_DN7
A36	PE3_RX_DP7	B36	PE3_TX_DP7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO16 Pin Definition [CPU2]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE3_RX_DP8	B2	PE3_TX_DP8
A3	PE3_RX_DN8	B3	PE3_TX_DN8
A4	GND	B4	GND
A5	PE3_RX_DN9	B5	PE3_TX_DN9
A6	PE3_RX_DP9	B6	PE3_TX_DP9
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSNT1
A13	GND	B13	GND
A14	PE3_RX_DP10	B14	PE3_TX_DP10
A15	PE3_RX_DN10	B15	PE3_TX_DN10
A16	GND	B16	GND
A17	PE3_RX_DN11	B17	PE3_TX_DN11
A18	PE3_RX_DP11	B18	PE3_TX_DP11
A19	GND	B19	GND
A20	PE3_RX_DP12	B20	PE3_TX_DP12
A21	PE3_RX_DN12	B21	PE3_TX_DN12
A22	GND	B22	GND
A23	PE3_RX_DN13	B23	PE3_TX_DN13
A24	PE3_RX_DP13	B24	PE3_TX_DP13
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSNT2
A31	GND	B31	GND
A32	PE3_RX_DP14	B32	PE3_TX_DP14
A33	PE3_RX_DN14	B33	PE3_TX_DN14
A34	GND	B34	GND
A35	PE3_RX_DN15	B35	PE3_TX_DN15
A36	PE3_RX_DP15	B36	PE3_TX_DP15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO17 Pin Definition [CPU2]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE5_RX_DN0	B2	PE5_TX_DN0
A3	PE5_RX_DP0	B3	PE5_TX_DP0
A4	GND	B4	GND
A5	PE5_RX_DN1	B5	PE5_TX_DN1
A6	PE5_RX_DP1	B6	PE5_TX_DP1
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSTNT1
A13	GND	B13	GND
A14	PE5_RX_DN2	B14	PE5_TX_DP2
A15	PE5_RX_DP2	B15	PE5_TX_DN2
A16	GND	B16	GND
A17	PE5_RX_DN3	B17	PE5_TX_DP3
A18	PE5_RX_DP3	B18	PE5_TX_DN3
A19	GND	B19	GND
A20	PE5_RX_DN4	B20	PE5_TX_DP4
A21	PE5_RX_DP4	B21	PE5_TX_DN4
A22	GND	B22	GND
A23	PE5_RX_DN5	B23	PE5_TX_DN5
A24	PE5_RX_DP5	B24	PE5_TX_DP5
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSTNT2
A31	GND	B31	GND
A32	PE5_RX_DN6	B32	PE5_TX_DN6
A33	PE5_RX_DP6	B33	PE5_TX_DP6
A34	GND	B34	GND
A35	PE5_RX_DN7	B35	PE5_TX_DN7
A36	PE5_RX_DP7	B36	PE5_TX_DP7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO18 Pin Definition [CPU2]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE5_RX_DN8	B2	PE5_TX_DN8
A3	PE5_RX_DP8	B3	PE5_TX_DP8
A4	GND	B4	GND
A5	PE5_RX_DN9	B5	PE5_TX_DN9
A6	PE5_RX_DP9	B6	PE5_TX_DP9
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSNT1
A13	GND	B13	GND
A14	PE5_RX_DN10	B14	PE5_TX_DN10
A15	PE5_RX_DP10	B15	PE5_TX_DP10
A16	GND	B16	GND
A17	PE5_RX_DN11	B17	PE5_TX_DN11
A18	PE5_RX_DP11	B18	PE5_TX_DP11
A19	GND	B19	GND
A20	PE5_RX_DN12	B20	PE5_TX_DP12
A21	PE5_RX_DP12	B21	PE5_TX_DN12
A22	GND	B22	GND
A23	PE5_RX_DN13	B23	PE5_TX_DN13
A24	PE5_RX_DP13	B24	PE5_TX_DP13
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSNT2
A31	GND	B31	GND
A32	PE5_RX_DN14	B32	PE5_TX_DN14
A33	PE5_RX_DP14	B33	PE5_TX_DP14
A34	GND	B34	GND
A35	PE5_RX_DN15	B35	PE5_TX_DN15
A36	PE5_RX_DP15	B36	PE5_TX_DP15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO19 Pin Definition [CPU2]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE4_RX_DN0	B2	PE4_TX_DP0
A3	PE4_RX_DP0	B3	PE4_TX_DN0
A4	GND	B4	GND
A5	PE4_RX_DN1	B5	PE4_TX_DP1
A6	PE4_RX_DP1	B6	PE4_TX_DN1
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSTNT1
A13	GND	B13	GND
A14	PE4_RX_DP2	B14	PE4_TX_DP2
A15	PE4_RX_DN2	B15	PE4_TX_DN2
A16	GND	B16	GND
A17	PE4_RX_DP3	B17	PE4_TX_DP3
A18	PE4_RX_DN3	B18	PE4_TX_DN3
A19	GND	B19	GND
A20	PE4_RX_DN4	B20	PE4_TX_DP4
A21	PE4_RX_DP4	B21	PE4_TX_DN4
A22	GND	B22	GND
A23	PE4_RX_DP5	B23	PE4_TX_DP5
A24	PE4_RX_DN5	B24	PE4_TX_DN5
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSTNT2
A31	GND	B31	GND
A32	PE4_RX_DP6	B32	PE4_TX_DP6
A33	PE4_RX_DN6	B33	PE4_TX_DN6
A34	GND	B34	GND
A35	PE4_RX_DP7	B35	PE4_TX_DP7
A36	PE4_RX_DN7	B36	PE4_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO20 Pin Definition [CPU2]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE4_RX_DP8	B2	PE4_TX_DP8
A3	PE4_RX_DN8	B3	PE4_TX_DN8
A4	GND	B4	GND
A5	PE4_RX_DP9	B5	PE4_TX_DP9
A6	PE4_RX_DN9	B6	PE4_TX_DN9
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSNT1
A13	GND	B13	GND
A14	PE4_RX_DP10	B14	PE4_TX_DP10
A15	PE4_RX_DN10	B15	PE4_TX_DN10
A16	GND	B16	GND
A17	PE4_RX_DP11	B17	PE4_TX_DP11
A18	PE4_RX_DN11	B18	PE4_TX_DN11
A19	GND	B19	GND
A20	PE4_RX_DN12	B20	PE4_TX_DP12
A21	PE4_RX_DP12	B21	PE4_TX_DN12
A22	GND	B22	GND
A23	PE4_RX_DN13	B23	PE4_TX_DP13
A24	PE4_RX_DP13	B24	PE4_TX_DN13
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSNT2
A31	GND	B31	GND
A32	PE4_RX_DN14	B32	PE4_TX_DP14
A33	PE4_RX_DP14	B33	PE4_TX_DN14
A34	GND	B34	GND
A35	PE4_RX_DP15	B35	PE4_TX_DP15
A36	PE4_RX_DN15	B36	PE4_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO21 Pin Definition [CPU2]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE1_RX_DN15	B2	PE1_TX_DP15
A3	PE1_RX_DP15	B3	PE1_TX_DN15
A4	GND	B4	GND
A5	PE1_RX_DN14	B5	PE1_TX_DN14
A6	PE1_RX_DP14	B6	PE1_TX_DP14
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSENT1
A13	GND	B13	GND
A14	PE1_RX_DP13	B14	PE1_TX_DP13
A15	PE1_RX_DN13	B15	PE1_TX_DN13
A16	GND	B16	GND
A17	PE1_RX_DP12	B17	PE1_TX_DN12
A18	PE1_RX_DN12	B18	PE1_TX_DP12
A19	GND	B19	GND
A20	PE1_RX_DN11	B20	PE1_TX_DP11
A21	PE1_RX_DP11	B21	PE1_TX_DN11
A22	GND	B22	GND
A23	PE1_RX_DN10	B23	PE1_TX_DN10
A24	PE1_RX_DP10	B24	PE1_TX_DP10
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSENT2
A31	GND	B31	GND
A32	PE1_RX_DP9	B32	PE1_TX_DP9
A33	PE1_RX_DN9	B33	PE1_TX_DN9
A34	GND	B34	GND
A35	PE1_RX_DP8	B35	PE1_TX_DP8
A36	PE1_RX_DN8	B36	PE1_TX_DN8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO22 Pin Definition [CPU2]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE1_RX_DN7	B2	PE1_TX_DP7
A3	PE1_RX_DP7	B3	PE1_TX_DN7
A4	GND	B4	GND
A5	PE1_RX_DN6	B5	PE1_TX_DP6
A6	PE1_RX_DP6	B6	PE1_TX_DN6
A7	GND	B7	GND
A8	BP IFDET1/CLKREQ#	B8	SMB_CLK1
A9	PCIE_WAKE	B9	SMB_DAT1
A10	GND	B10	GND
A11	REFCLK_DP	B11	PERST1
A12	REFCLK_DN	B12	PRSNT1
A13	GND	B13	GND
A14	PE1_RX_DN5	B14	PE1_TX_DP5
A15	PE1_RX_DP5	B15	PE1_TX_DN5
A16	GND	B16	GND
A17	PE1_RX_DN4	B17	PE1_TX_DN4
A18	PE1_RX_DP4	B18	PE1_TX_DP4
A19	GND	B19	GND
A20	PE1_RX_DP3	B20	PE1_TX_DN3
A21	PE1_RX_DN3	B21	PE1_TX_DP3
A22	GND	B22	GND
A23	PE1_RX_DP2	B23	PE1_TX_DN2
A24	PE1_RX_DN2	B24	PE1_TX_DP2
A25	GND	B25	GND
A26	BP IFDET2/PWRBRK#	B26	SMB_CLK2
A27	PCIE_WAKE	B27	SMB_DAT2
A28	GND	B28	GND
A29	REFCLK_DP	B29	PERST2
A30	REFCLK_DN	B30	PRSNT2
A31	GND	B31	GND
A32	PE1_RX_DN1	B32	PE1_TX_DP1
A33	PE1_RX_DP1	B33	PE1_TX_DN1
A34	GND	B34	GND
A35	PE1_RX_DN0	B35	PE1_TX_DP0
A36	PE1_RX_DP0	B36	PE1_TX_DN0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

2.7 Dr. Debug

Dr. Debug is used to provide code information, which makes troubleshooting even easier. Please see the diagrams below for reading the Dr. Debug codes.

Code	Description
0x10	PEI_CORE_STARTED
0x11	PEI_CAR_CPU_INIT
0x15	PEI_CAR_NB_INIT
0x19	PEI_CAR_SB_INIT
0x31	PEI_MEMORY_INSTALLED
0x32	PEI_CPU_INIT
0x33	PEI_CPU_CACHE_INIT
0x34	PEI_CPU_AP_INIT
0x35	PEI_CPU_BSP_SELECT
0x36	PEI_CPU_SMM_INIT
0x37	PEI_MEM_NB_INIT
0x3B	PEI_MEM_SB_INIT
0x4F	PEI_DXE_IPL_STARTED
0x60	DXE_CORE_STARTED
0x61	DXE_NVRAM_INIT

0x62 DXE_SBRUN_INIT

0x63 DXE_CPU_INIT

0x68 DXE_NB_HB_INIT

0x69 DXE_NB_INIT

0x6A DXE_NB_SMM_INIT

0x70 DXE_SB_INIT

0x71 DXE_SB_SMM_INIT

0x72 DXE_SB_DEVICES_INIT

0x78 DXE_ACPI_INIT

0x79 DXE_CSM_INIT

0x90 DXE_BDS_STARTED

0x91 DXE_BDS_CONNECT_DRIVERS

0x92 DXE_PCI_BUS_BEGIN

0x93 DXE_PCI_BUS_HPC_INIT

0x94 DXE_PCI_BUS_ENUM

0x95 DXE_PCI_BUS_REQUEST_RESOURCES

0x96 DXE_PCI_BUS_ASSIGN_RESOURCES

0x97 DXE_CON_OUT_CONNECT

0x98	DXE_CON_IN_CONNECT
0x99	DXE_SIO_INIT
0x9A	DXE_USB_BEGIN
0x9B	DXE_USB_RESET
0x9C	DXE_USB_DETECT
0x9D	DXE_USB_ENABLE
0xA0	DXE_IDE_BEGIN
0xA1	DXE_IDE_RESET
0xA2	DXE_IDE_DETECT
0xA3	DXE_IDE_ENABLE
0xA4	DXE_SCSI_BEGIN
0xA5	DXE_SCSI_RESET
0xA6	DXE_SCSI_DETECT
0xA7	DXE_SCSI_ENABLE
0xA8	DXE_SETUP_VERIFYING_PASSWORD
0xA9	DXE_SETUP_START
0xAB	DXE_SETUP_INPUT_WAIT
0xAD	DXE_READY_TO_BOOT

0xAE	DXE_LEGACY_BOOT
0xAF	DXE_EXIT_BOOT_SERVICES
0xB0	RT_SET_VIRTUAL_ADDRESS_MAP_BEGIN
0xB1	RT_SET_VIRTUAL_ADDRESS_MAP_END
0xB2	DXE_LEGACY_OPROM_INIT
0xB3	DXE_RESET_SYSTEM
0xB4	DXE_USB_HOTPLUG
0xB5	DXE_PCI_BUS_HOTPLUG
0xB6	DXE_NVRAM_CLEANUP
0xB7	DXE_CONFIGURATION_RESET
0xF0	PEI_RECOVERY_AUTO
0xF1	PEI_RECOVERY_USER
0xF2	PEI_RECOVERY_STARTED
0xF3	PEI_RECOVERY_CAPSULE_FOUND
0xF4	PEI_RECOVERY_CAPSULE_LOADED
0xE0	PEI_S3_STARTED
0xE1	PEI_S3_BOOT_SCRIPT

0xE2	PEI_S3_VIDEO_REPOST
0xE3	PEI_S3_OS_WAKE
0x50	PEI_MEMORY_INVALID_TYPE
0x53	PEI_MEMORY_NOT_DETECTED
0x55	PEI_MEMORY_NOT_INSTALLED
0x57	PEI_CPU_MISMATCH
0x58	PEI_CPU_SELF_TEST_FAILED
0x59	PEI_CPU_NO_MICROCODE
0x5A	PEI_CPU_ERROR
0x5B	PEI_RESET_NOT_AVAILABLE
0xD0	DXE_CPU_ERROR
0xD1	DXE_NB_ERROR
0xD2	DXE_SB_ERROR
0xD3	DXE_ARCH_PROTOCOL_NOT_AVAILABLE
0xD4	DXE_PCI_BUS_OUT_OF_RESOURCES
0xD5	DXE_LEGACY_OPROM_NO_SPACE
0xD6	DXE_NO_CON_OUT

0xD7	DXE_NO_CON_IN
0xD8	DXE_INVALID_PASSWORD
0xD9	DXE_BOOT_OPTION_LOAD_ERROR
0xDA	DXE_BOOT_OPTION_FAILED
0xDB	DXE_FLASH_UPDATE_FAILED
0xDC	DXE_RESET_NOT_AVAILABLE
0xE8	PEI_MEMORY_S3_RESUME_FAILED
0xE9	PEI_S3_RESUME_PPI_NOT_FOUND
0xEA	PEI_S3_BOOT_SCRIPT_ERROR
0xEB	PEI_S3_OS_WAKE_ERROR

2.8 Identification Purpose Switches

Unit Identification
Switch/LED
(UID1)



Use the UID button to locate the server working on behind a rack of servers.

When the UID button on the front or rear panel is pressed, the front/rear UID blue LED indicator will be truned on. Press the UID button again to turn off the indicator.

Power Switch/LED
(PWR_BTN)



Power Switch allows users to quickly turn on/off the system. When the power button is on, the green LED indicator will be truned on.



1. Press and hold the UID button for 4 seconds, BMC will trigger an external reset.
2. Press and hold the UID button for 10 seconds, BMC will reset and load default values.

2.9 Replacing the CMOS Battery



1. Ensure the battery is installed before unplugging the power cord or installing/removing the motherboard.
2. Always turn off the computer and unplug the power cord before replacing the battery.
3. For safety, please replace the battery with the same or equivalent type recommended by the manufacturer.
4. Dispose of the used batteries in accordance with local regulations.

Refer to the section **1.4 Motherboard Layout** to locate the battery.

**The illustration is for reference only. The actual installation may be slightly different by socket design.*

Step 1

Shut down and unplug the computer.

Flat: Gently press the socket clip.

Upright: Gently push the socket clip away from the battery.

Step 2

Flat: Remove the battery when it pops up. Or press down on one end of the battery to pop it up and remove it.

Upright: Remove the battery.

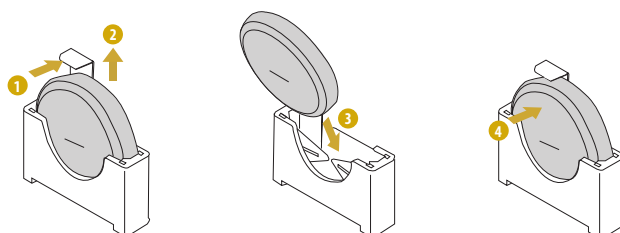
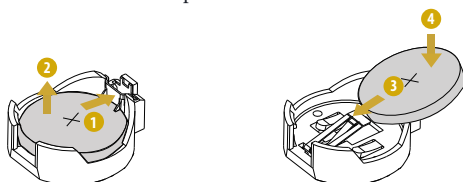
Step 3

Flat: Insert a new battery into the socket with the positive side (+ sign) facing up.

Upright: Insert a new battery into the socket with the positive side (+ sign) facing the open side of the socket clip.

Step 4

Press the battery down until it clicks into place.



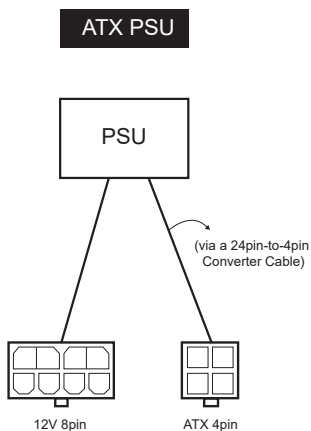
Replacing the Wired CMOS Battery

To replace a wired CMOS battery, completely power down the computer and unplug it from the power source. Locate the old battery, carefully trace its wires to the small connector on the motherboard, and unplug it. Install a new battery in its place and connect it to the motherboard.

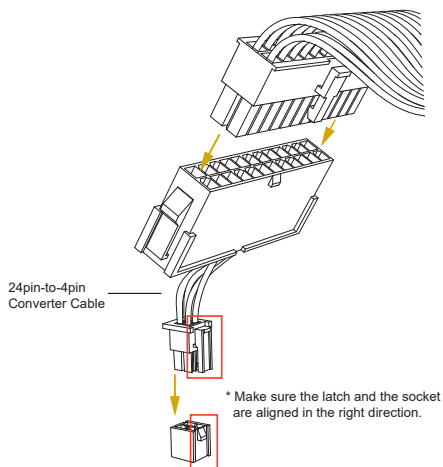


2.10 ATX PSU Power Connections

This motherboard supports ATX power input. Please refer to the table below for the required connections between the motherboard and the power supply.



The following diagram illustrates how to connect the bundled ATX 24pin-to-4pin converter cable.



2.11 Dual LAN and Teaming Operation Guide

Dual LAN with Teaming enabled on this motherboard allows two single connections to act as one single connection(s) for twice the transmission bandwidth, making data transmission more effective and improving the quality of transmission of distant images. Fault tolerance on the dual LAN network prevents network downtime by transferring the workload from a failed port to a working port.



The speed of transmission is subject to the actual network environment or status even with Teaming enabled.

Before setting up Teaming, please make sure whether the Switch (or Router) supports Teaming (IEEE 802.3ad Link Aggregation). Specify a preferred adapter in Intel PROSet. Under normal conditions, the Primary adapter handles all non-TCP/IP traffic. The Secondary adapter will receive fallback traffic if the primary fails. If the Preferred Primary adapter fails, but is later restored to an active status, control is automatically switched back to the Preferred Primary adapter.

Step 1

From **Device Manager**, open the properties of a team.

Step 2

Click the **Settings** tab.

Step 3

Click the **Modify Team** button.

Step 4

Select the adapter to the primary adapter and click the **Set Primary** button.

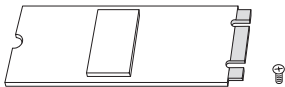
If it does not specify a preferred primary adapter, the software will choose an adapter of the highest capability (model and speed) to act as the default primary. If a failover occurs, another adapter becomes the primary. The adapter will, however, rejoin the team as a non-primary.

2.12 M.2 SSD Module Installation Guide

The M.2 Socket (M2_1/M2_2, Key M) supports type 2280/22110 M.2 PCI Express module up to Gen5 x4 or Gen5 x2.

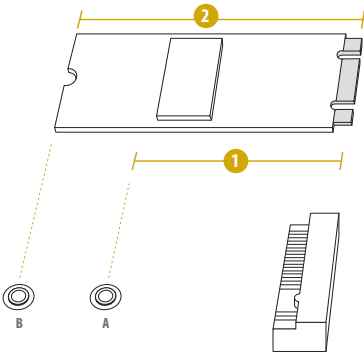
**M2_1 only supports PCIe5.0 x2 when RDS2 is linked to NVSwitch.*

Installing the M.2 SSD Module



Step 1

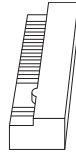
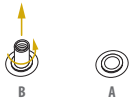
Prepare a M.2 SSD module and the screw.



Step 2

Depending on the PCB type and length of the M.2 SSD module, find the corresponding nut location to be used.

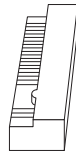
No.	1	2
Nut Location	A (NUT_80_1/2)	B (NUT_110_1/2)
PCB Length	8 cm	11 cm
Module Type	Type 2280	Type 22110

**Step 3**

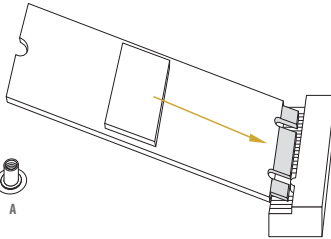
Move the standoff based on the module type and length.

Skip Step 3 and 4 and go straight to Step 5 if using the default nut.

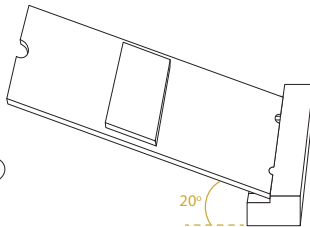
Otherwise, release the standoff by hand.

**Step 4**

Peel off the yellow protective film on the nut to be used. Hand tighten the standoff into the desired nut location on the motherboard.

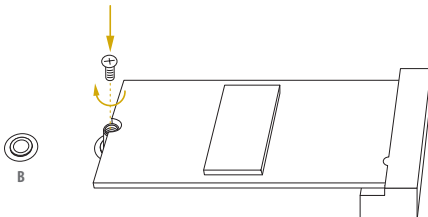
**Step 5**

Align and gently insert the M.2 SSD module into the M.2 slot. Please be aware that the M.2 SSD module only fits in one orientation.

**Step 6**

Tighten the screw with a screwdriver to secure the module into place.

Please do not overtighten the screw as this might damage the module.



Chapter 3 UEFI Setup Utility

3.1 Introduction

This section explains how to use the UEFI SETUP UTILITY to configure the system. The UEFI chip on the motherboard stores the UEFI SETUP UTILITY. Run the UEFI SETUP UTILITY when starting up the computer. Please press <F2> or during the Power-On-Self-Test (POST) to enter the UEFI SETUP UTILITY; otherwise, POST will continue with its test routines.

Restart the system by pressing <Ctrl> + <Alt> + <Delete> to enter the UEFI SETUP UTILITY after POST, or by pressing the reset button on the system chassis. This allows user to restart by turning the system off and then back on.



Because the UEFI software is constantly being updated, the following UEFI setup screens and descriptions are for reference purpose only, and they may not exactly match what seeing on the screen.

3.1.1 UEFI Menu Bar

The top of the screen has a menu bar with the following selections:

Item	Description
Main	To set up the system time/date information
Advanced	To set up the advanced UEFI features
Server Mgmt	To manage the server
Event Logs	For event log configuration
Security	To set up the security features
Boot	To set up the default system device to locate and load the Operating System
Exit	To exit the current screen or the UEFI SETUP UTILITY

Use <←> key or <→> key to choose among the selections on the menu bar, and then press <Enter> to get into the sub screen.

3.1.2 Navigation Keys

Please check the following table for the function description of each navigation key.

Navigation Key(s)	Function Description
← / →	Moves cursor left or right to select Screens
↑ / ↓	Moves cursor up or down to select items
+ / -	To change option for the selected items
<Tab>	Switch to next function
<Enter>	To bring up the selected screen
<PGUP>	Go to the previous page
<PGDN>	Go to the next page
<HOME>	Go to the top of the screen
<END>	Go to the bottom of the screen
<F1>	To display the General Help Screen
<F7>	Discard changes and exit the UEFI SETUP UTILITY
<F9>	Load optimal default values for all the settings
<F10>	Save changes and exit the UEFI SETUP UTILITY
<F12>	Print screen
<ESC>	Jump to the Exit Screen or exit the current screen

3.2 Main Screen

Once entering the UEFI SETUP UTILITY, the Main screen will appear and display the system overview. The Main screen provides system overview information and allows user to set the system time and date.



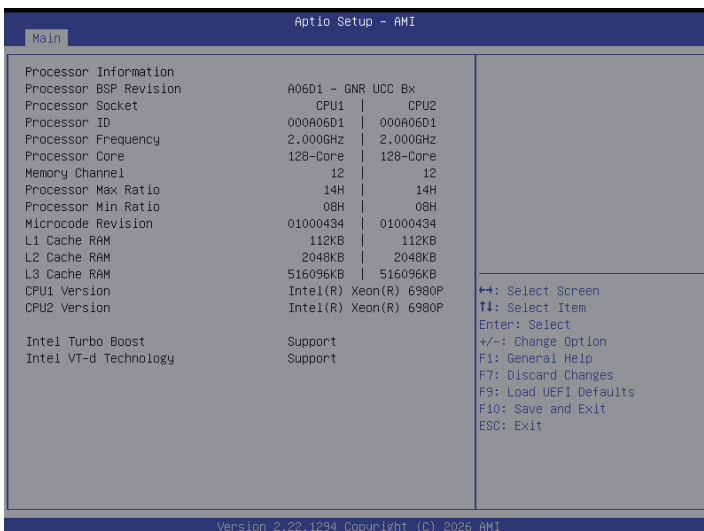
3.2.1 Motherboard Information

Press [Enter] to view the information of the motherboard.



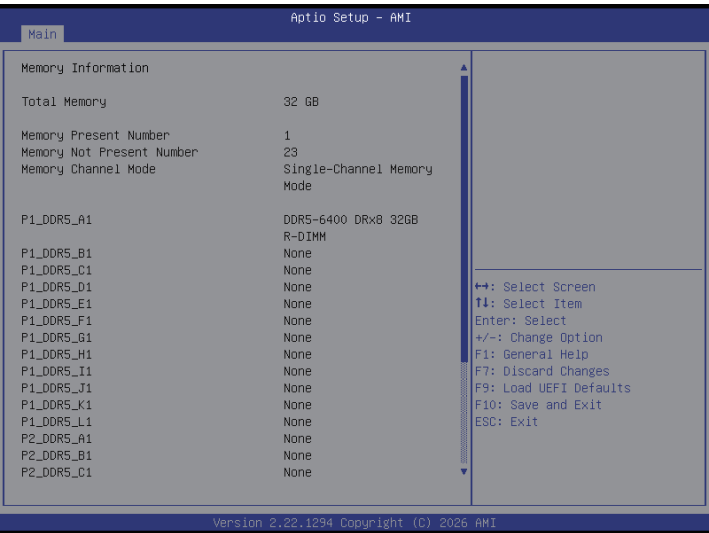
3.2.2 Processor Information

Press [Enter] to view the information of the processor.



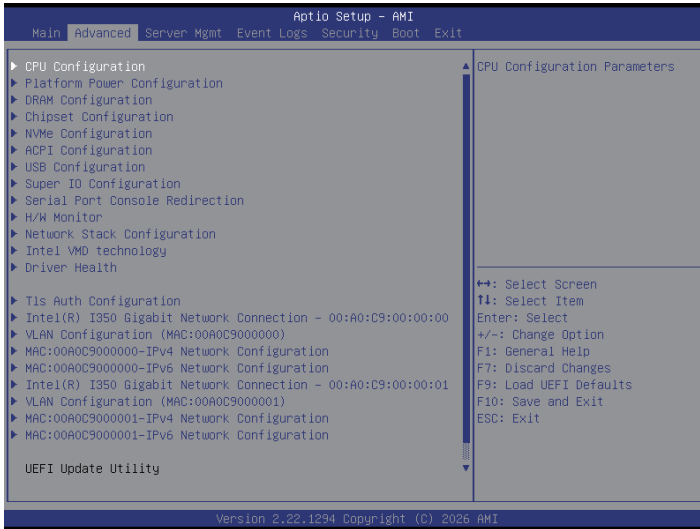
3.2.3 Memory Information

Press [Enter] to view the information of the memory.



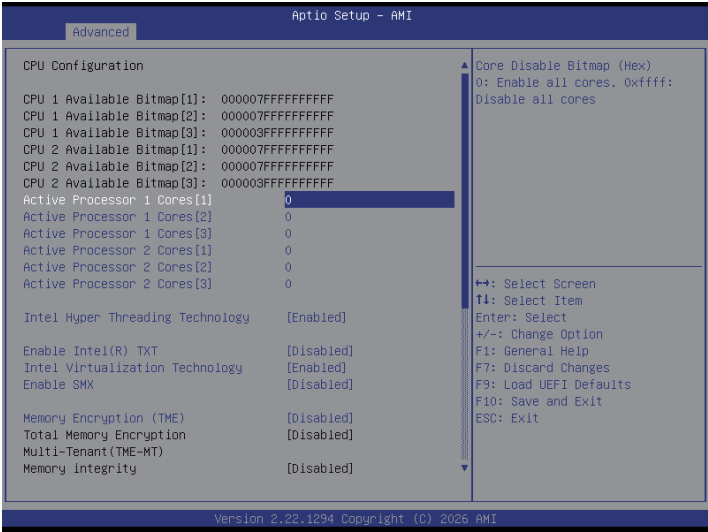
3.3 Advanced Screen

In this section, set the configurations for the following items: CPU Configuration, Platform Power Configuration, DRAM Configuration, Chipset Configuration, NVMe Configuration, ACPI Configuration, USB Configuration, Super IO Configuration, Serial Port Console Redirection, H/W Monitor, Network Stack Configuration, Intel VMD Technology, Driver Health, Tls Auth Configuration and Instant Flash.



Setting wrong values in this section may cause the system to malfunction.

3.3.1 CPU Configuration



Active Processor 1/2 Cores

Core Disable Bitmap (Hex)

0: Enable all cores.

0xffff: Disable all cores

Intel Hyper Threading Technology

Intel Hyper Threading Technology allows multiple threads to run on each core, so that the overall performance on threaded software is improved.

Enable Intel TXT

Use this item to enable Intel Trusted Execution Technology Configuration.

Intel Virtualization Technology

Intel Virtualization Technology allows a platform to run multiple operating systems and applications in independent partitions, so that one computer system can function as multiple virtual systems.

Enable SMX

Use this item to enable Safer Mode Extensions.

Memory Encryption (TME)

Use this item to enable or disable Memory Encryption (TME).

Total Memory Encryption Multi-Tenant (TME-MT)

Use this item to enable or disable Total Memory Encryption-Multi-Tenant (TME-MT). Can be enabled only if Socket Configuration -> Porcessor Configuration -> Limit CPU PA to 46 bits=Disable.

Memory Integrity

Use this item to enable or disable memory integrity.

TME Encryption Algorithm

Choose Encryption Algorithm to be used for Total Memory Encryption (TME).

Trust Domain Extension (TDX)

Use this item to enable or disable Trust Domain Extension (TDX).

TDX Secure Arbitration Mode Loader (SEAM Loader)

Use this item to enable or disable TDX Secure Arbitration Mode Loader (SEAM Loader).

SGX Factory Reset

Perform SGX Factory Reset, on subsequent boot: delete all registration data, if SGX enabled will force Initial Platform Establishment flow.

SW Guard Extensions (SGX)

Use this item to enable or disable Software Guard Extensions (SGX).

SGX Package Info In-Band Access

Use this item to enable or disable Software Guard Extensions (SGX) Package Info In-Band Access.

SGX PRMRR Size Requested

Use this item to select the SGX PRMRR Size per domain.

SGX QoS

Use this item to enable or disable SGX Quality of Service.

Select Owner EPOCH input type

Each EPOCH is 64bit, keys value should be different than 0. After generating new epoch via 'Change to New Random Owner EPOCHs', the selection reverts back to 'Manual User Defined Owner EPOCHs'. In next boot keys will be hidden and state will be 'SGX Owner EPOCH activated'.

SGXLEPUBKEYHASHx Write Enable

Select this item to Enable write to SGXLEPUBKEYHASH[3..0] from OS/SW.

SGX Auto MP Registration

Use this item to enable or disable automatic registration in OS MPA agent.

SGX Registration Server

Use this item to choose which server should be used for SGX registration.

Disable ACTM Launch

Use this item to disable ACTM Launch.

DCU Streamer Prefetcher

DCU streamer prefetcher is an L1 data cache prefetcher (MSR 1A4h [2]).

LLC Prefetch

Use this item to enable or diable LLC Prefetch on all threads.

Hardware Prefetcher

Automatically prefetch data and code for the processor. Enable for better performance.

Adjacent Cache Line Prefetch

Automatically prefetch the subsequent cache line while retrieving the currently requested cache line. Enable for better performance.

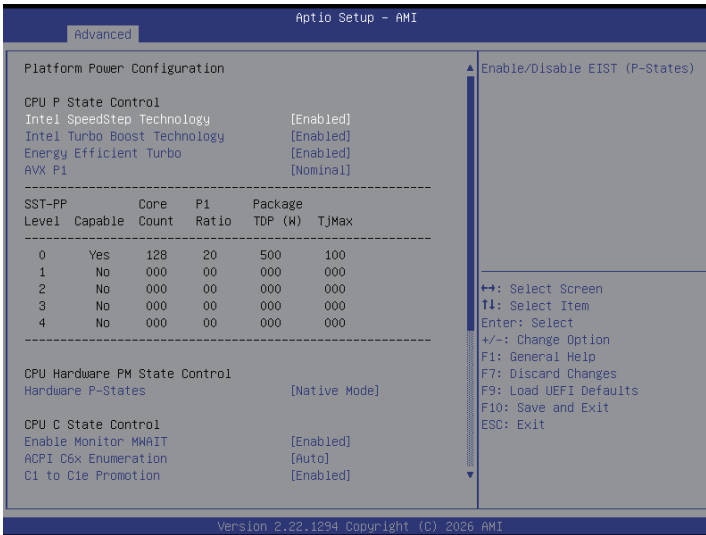
AES-NI

Use this item to enable or disable AES-NI support.

SNC

Use this item to enable or disable SNC mode. Configure this item to Disable, BIOS will enable UMA mode. Number of clusters is determined by BIOS based on detected SKU.

3.3.2 Platform Power Configuration



Intel SpeedStep Technology

Intel SpeedStep technology allows processors to switch between multiple frequencies and voltage points for better power saving and heat dissipation. CPU turbo ratio can be fixed when Intel SpeedStep Technology set Disabled and Intel Turbo Boost Technology set Enabled.



Please note that enabling this function may reduce CPU voltage and lead to system stability or compatibility issues with some power supplies. Please set this item to [Disabled] if above issues occur.

Intel Turbo Boost Technology

Intel Turbo Boost Technology enables the processor to run above its base operating frequency when the operating system requests the highest performance state.

Energy Efficient Turbo

Select this item to enable or disable Energy Efficient Turbo.

Enable: MSR 0x1FC Bit[19] = 0.

Disable: MSR 0x1FC Bit[19] = 1.

AVX P1

Select this item to configure AVX P1 level.

Hardware P-States

This item supports below selections:

Disable: Hardware chooses a P-state based on OS Request (Legacy P-States).

Native Mode: Hardware chooses a P-state based on OS guidance.

Out of Band Mode: Hardware autonomously chooses a P-state (no OS guidance)

Native Mode with No Legacy Support: Hardware autonomously chooses a P-state based on OS guidance with no legacy support.

Enable Monitor MWAIT

Select this item to configure Monitor and MWAIT instructions whether Auto maps to enable.

ACPI C6x Enumeration

Auto: Maps to C6-P as ACPI C2.

Disable: Don't enumerate any C6 state in ACPI

C6 as ACPI C2/C3: Enumerate C6 as ACPI C2/C3 state. PkgC6 is not allowed.

C6-P as ACPI C2/C3: Enumerate C6-P as ACPI C2/C3 state. PkgC6 is allowed.

C1 to Cle Promotion

CPU will promote C1 request to Cle state.

Package C State

Package C State limit, the state Auto maps is program specific.

Power Performance Tuning

Use this item to decides which controls EPB.

OS Controls EPB: Specifies IA32_ENERGY_PERF_BIAS is used.

BIOS Controls EPB: Specifies ENERGY_PERF_BIAS_CONFIG is used.

PECI Controls EPB: Specifies PCS53 is used.

ENERGY_PERF_BIAS_CFG mode

Use this item to use input from ENERGY_PERF_BIAS_CONFIG mode selection. PERF/Balanced, Perf/Balanced or Power/Power.

PL1 Power Limit

PL1 Power Limit is in Watts and the value may vary from 0 to Fused Value. If the value is 0, the fused value will be programmed. A value greater than fused TDP value will not be programmed.

PL1 Time Window

PL1 value in seconds. The value may vary from 1 to 5. Indicates the time window over which TDP value should be maintained.

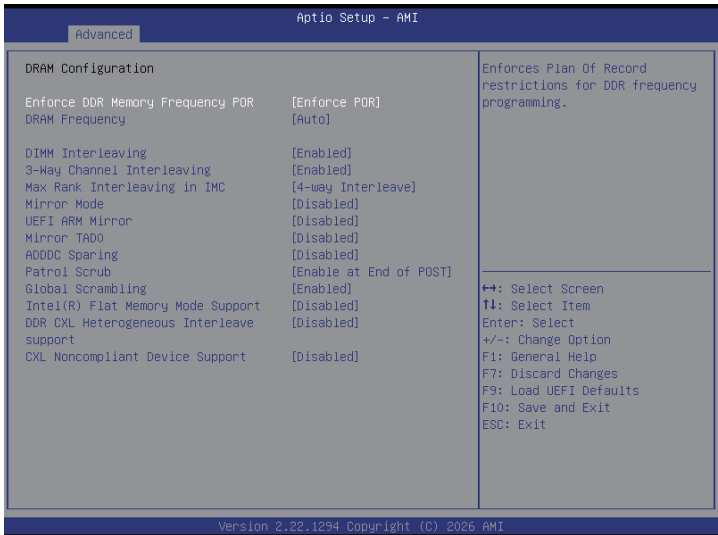
PL2 Power Limit

PL2 Power Limit in Watts. The value may vary from 0 to 120% Fused TDP Value. If the value is 0, BIOS programs $120\% * \text{Fused TDP value}$.

PL2 Time Window

PL2 value in seconds. The value may vary from 0.012 to 0.039. Indicates the time window over which TDP value should be maintained.

3.3.3 DRAM Configuration



Enforce DDR Memory Frequency POR

Enable to enforce POR restrictions for DDR frequency and voltage programming.

DRAM Frequency

Maximum Host DDR Memory Frequency Selections in MT/s. If the [Auto] is selected, a frequency is chosen automatically based on the minimum tCK given by the SPD. If enforce POR is disabled, user fwill be able to run at higher frequencies than the memory support (limited by processor support).

DIMM Interleaving

Enable this item to allow interleaving to be performed at the highest possible MC * Channel interleaving ways. Or disable this item to enforce interleaving to only 1-way.

3-Way Channel Interleaving

Enable this item to allow 3-way channel interleaving. Or disable this item to default to number of channels available per MC when DIMM interleaving is enabled.

Max Rank Interleaving in IMC

Use this item to select Rank Interleaving setting.

Mirror Mode

Full Mirror Mode will set entire 1LM memory in system to be mirrored, consequently reducing the memory capacity by half. Partial Mirror Mode will enable the required size of memory to be mirrored. If rank sparing is enabled partial mirroring will not take effect. Enabling any type of Mirror Mode will disable XPT Prefetch.

UEFI ARM Mirror

Imitate behavior of UEFI based Address Range Mirror with setup option.

Mirror TAD0

Enable Mirror on entire memory for TAD0.

ARM Mirror Percentage

Enter the percentage to be mirrored in basis points. Mirror options are 10%, 15%, 20%, 25%, 30%, 35%, 40%. 25% is represented 2500. Any other number entered will be rounded to nearest greater number, for ex. number > 2000 and <=2500 will be rounded to 2500. And any number >4000, will be rounded to 4000.

ADDDC Sparing

Enable or disable Memory Rank Sparing.

Patrol Scrub

Patrol Scrub is a background activity initiated by the processor to seek out and fix memory errors.

Data Scrambling for DDR4/5

Enable: Enables data scrambling for DDR4 and DDR5.

Disable: Disables this feature.

Auto: Sets it to the MRC default setting; current default is Enable.

Global Scrambling

Enable: Enables global data scrambling.

Disable: Disables this feature.

Intel(R) Flat Memory Mode Support

Enable or disable Intel(R) Flat Memory Mode support.

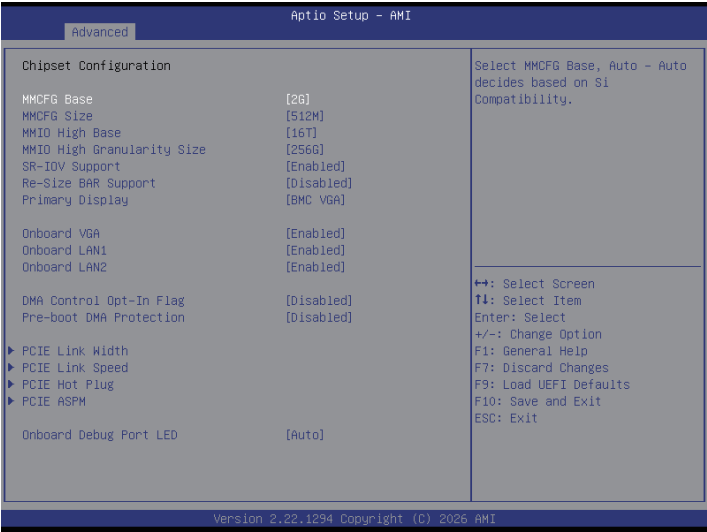
DDR CXL Heterogeneous Interleave support

Use this item to enable DDR CXL Heterogeneous Interleave support.

CXL Heterogeneous Device support

Use this item to enable or disable CXL Noncompliant Device Support.

3.3.4 Chipset Configuration



MMCFG Base

Use this item to select MMCFG Base. Auto-Auto decides based on Si compatibility.

MMCFG Size

Use this item to select MMCFG Size. Auto-Auto decides based on Si compatibility.

MMIO High Base

Use this item to select MMIO High Base.

MMIO High Granularity Size

Selects the allocation size used to assign mmioh resources. Per stack mmioh resource assignments are multiples of the granularity where 1 unit per stack is the default allocation.

SR-IOV Support

If system has SR-IOV capable PCIE Devices, this option Enables or Disables Single Root IO Virtualization Support.

Re-Size BAR Support

Enable or disable this item to Re-Size BAR supported upon the sysem has resizable BAR capable PCIE Devices.

Primary Display

Select which Graphics device as the Primary Display.

Onboard VGA

Use this to enable or disable the Onboard VGA function.

Onboard LAN1

Use this to enable or disable the Onboard LAN1 function.

Onboard LAN2

Use this to enable or disable the Onboard LAN2 function.

DMA Control Opt-In Flag

Select this item to enable DMA_CTRL_PLATFORM_OPT_IN_FLAG in the DMAR of the ACPI to request OS to enable DMA protection. Not compatible with Direct Device Assignment (DDA).

Pre-boot DMA Protection

Select this item to enable DMA Protection in Pre-boot Environment.

PCIe Link Width

Select this item to configure PCIe Link Width.

MCIO1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20/21/22 Link Width

Select PCIe Link Width for MCIO. The default value is Auto - x4x4x4x4. Options: Auto, x4x4x4x4, x4x4x8, x8x4x4, x8x8 and x16.

PCIe Link Speed

Select PCIe Link Speed.

MCIO1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20/21/22 Link Speed

Select PCIe Link Speed for MCIO. The default value is Auto - up to Gen5 (32GT/s).

M2_1/2_2 Link Speed

Select PCIe Link Speed for M.2. The default value is Auto - up to Gen5 (32GT/s).

PCIE Hot Plug

Select this item to configure PCIE Hot Plug globally.

MCIO1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20/21/22 Surprise Hot Plug

Enable or disable MCIO Surprise Hot Plug.

PCIE ASPM

Select this item to configure the PCIE ASPM.

ASPM Support (Global)

Select this item to disable ASPM Support in all PCIE root ports.

MCIO1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20/21/22 ASPM Support

Enables or disables the ASPM support in PCIE root port. Select [Auto] for the default value.

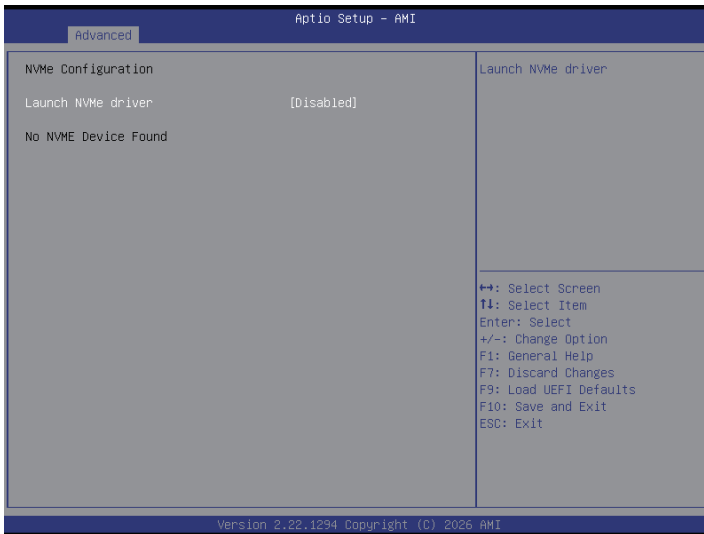
M2_1/2_2 ASPM Support

Enables or disables the ASPM support in PCIE root port. Select [Auto] for the default value.

Onboard Debug Port LED

Enable or disable the onboard Dr. Debug LED.

3.3.5 NVMe Configuration



Launch NVMe driver

Select this item to enable or disable launch NVMe driver.

3.3.6 ACPI Configuration



PCIE Devices Power On

Allow the system to be waked up by a PCIE device and enable wake on LAN.

RTC Alarm Power On

Use this item to enable or disable RTC (Real Time Clock) to power on the system.

RTC Alarm Hour

Use this item to set Hour of RTC power on feature.

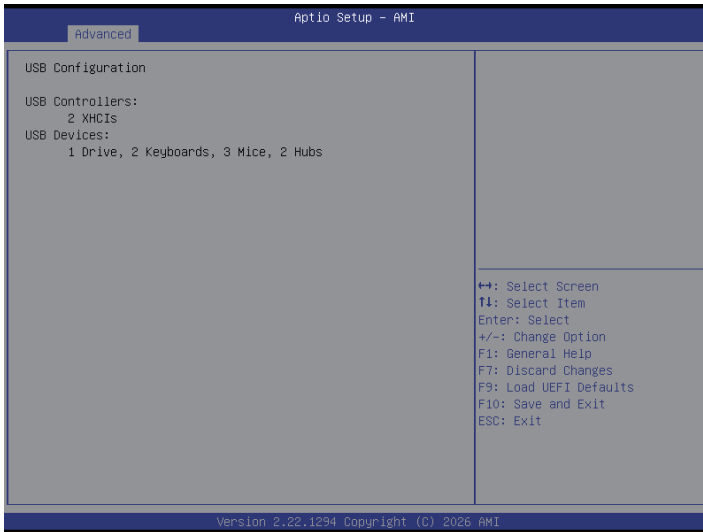
RTC Alarm Minute

Use this item to set Minute of RTC power on feature.

RTC Alarm Second

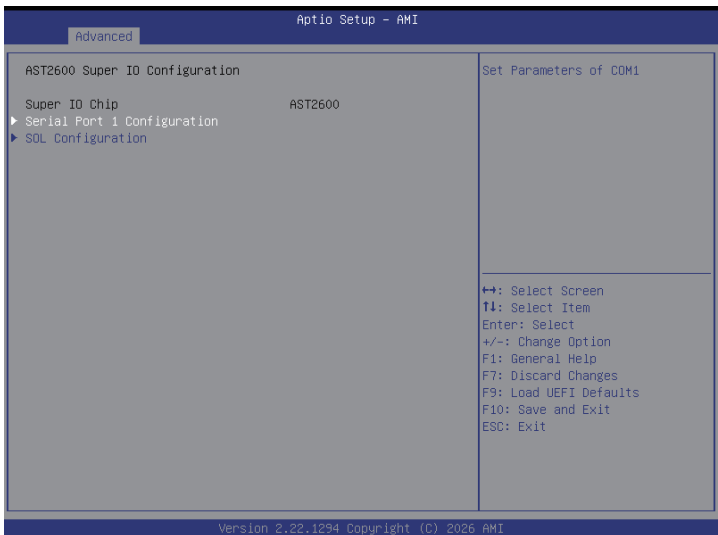
Use this item to set Second of RTC power on feature.

3.3.7 USB Configuration



The USB Configuration displays the USB Controllers and USB Devices informations.

3.3.8 Super IO Configuration



Serial Port 1 Configuration

Use this item to set parameters of COM1.

Serial Port

Use this item to enable or disable the serial port.

Change Settings

Use this item to select an optimal setting for Super IO device.

SOL Configuration

Use this item to set parameters of SOL.

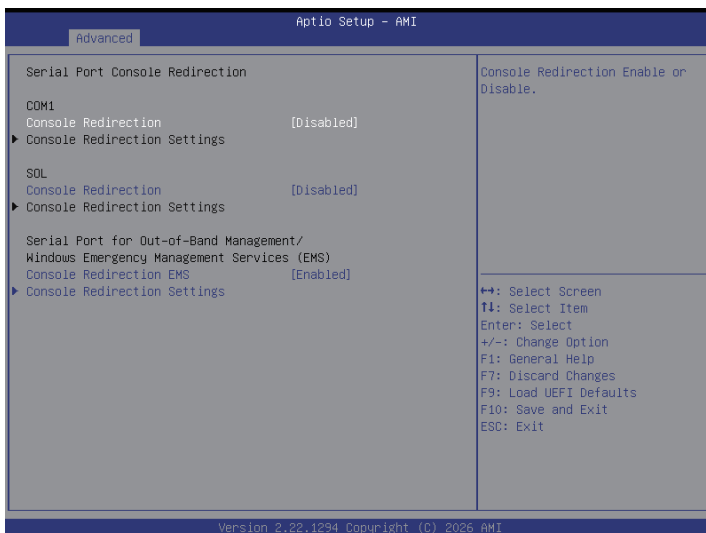
SOL Port

Use this item to set parameters of SOL.

Change Settings

Use this item to select an optimal setting for Super IO device.

3.3.9 Serial Port Console Redirection



COM1 / SOL

Console Redirection

Use this option to enable or disable Console Redirection. If this item is set to Enabled, it allows user to select a COM Port to be used for Console Redirection.

Console Redirection Settings

Use this option to configure Console Redirection Settings, and specify how the computer and the host computer to which are connected exchange information. Both computers should have the same or compatible settings.

Terminal Type

Use this item to select the preferred terminal emulation type for out-of-band management. It is recommended to select [VT-UTF8].

Option	Description
VT100	ASCII character set
VT100Plus	Extended VT100 that supports color and function keys
VT-UTF8	UTF8 encoding is used to map Unicode chars onto 1 or more bytes
ANSI	Extended ASCII character set

Bits Per Second

Use this item to select the serial port transmission speed. The speed used in the host computer and the client computer must be the same. Long or noisy lines may require lower transmission speed. The options include [9600], [19200], [38400], [57600] and [115200].

Data Bits

Use this item to set the data transmission size. The options include [7] and [8] (Bits).

Parity

Use this item to select the parity bit. The options include [None], [Even], [Odd], [Mark] and [Space].

Stop Bits

The item indicates the end of a serial data packet. The standard setting is [1] Stop Bit. Select [2] Stop Bits for slower devices.

Flow Control

Use this item to set the flow control to prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a "stop" signal can be sent to stop the data flow. Once the buffers are empty, a "start" signal can be sent to restart the flow. Hardware flow uses two wires to send start/stop signals. The options include [None] and [Hardware RTS/CTS].

VT-UTF8 Combo Key Support

Use this item to enable or disable the VT-UTF8 Combo Key Support for ANSI/VT100 terminals.

Recorder Mode

Use this item to enable or disable Recorder Mode to capture terminal data and send it as text messages.

Resolution 100x31

Use this item to enable or disable extended terminal resolution support.

Putty Keypad

Use this item to select Function Key and Keypad on Putty.

Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS)

Console Redirection EMS

Use this option to enable or disable Console Redirection. If this item is set to Enabled, it allows user to select a COM Port to be used for Console Redirection.

Console Redirection Settings

Use this option to configure Console Redirection Settings, and specify how the computer and the host computer to which are connected exchange information.

Out-of-Band Mgmt Port

Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.

Terminal Type EMS

Use this item to select the preferred terminal emulation type for out-of-band management. It is recommended to select [VT-UTF8].

Option	Description
VT100	ASCII character set
VT100+	Extended VT100 that supports color and function keys
VT-UTF8	UTF8 encoding is used to map Unicode chars onto 1 or more bytes
ANSI	Extended ASCII character set

Bits Per Second EMS

Use this item to select the serial port transmission speed. The speed used in the host computer and the client computer must be the same. Long or noisy lines may require lower transmission speed. The options include [9600], [19200], [57600] and [115200].

Flow Control EMS

Use this item to set the flow control to prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a "stop" signal can be sent to stop the data flow. Once the buffers are empty, a "start" signal can be sent to restart the flow. Hardware flow uses two wires to send start/stop signals. The options include [None], [Hardware RTS/CTS], and [Software Xon/Xoff].

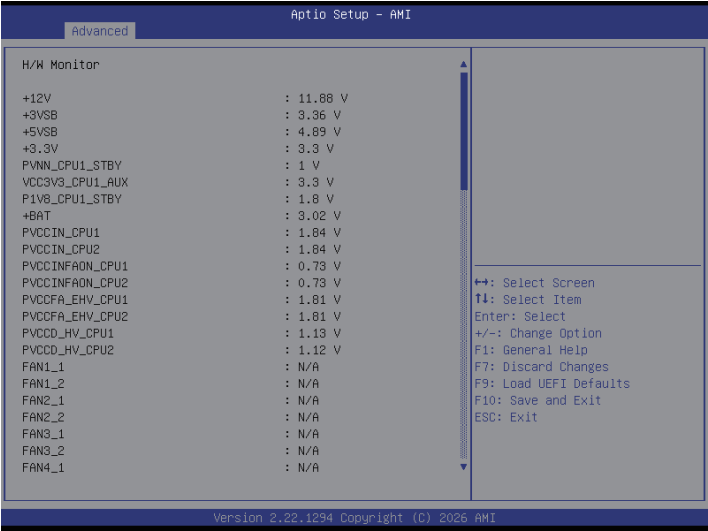
Data Bits EMS

Parity EMS

Stop Bits EMS

3.3.10 H/W Monitor

In this section, it allows user to monitor the status of the hardware on the system, including the parameters of the CPU temperature, motherboard temperature, CPU fan speed, chassis fan speed, and the critical voltage.



3.3.11 Network Stack Configuration



Network Stack

Enable UEFI network stack can prevents to perform from the single-user network boots and network installation. If disabled, the host does not use the network interface.

IPv4 PXE Support

Enable IPv4 PXE Boot support. If disabled, IPv4 PXE Boot Option is not supported.

IPv4 HTTP Support

Enable IPv4 HTTP Boot support. If disabled, IPv4 HTTP Boot Option is not supported.

IPv6 PXE Support

Enable IPv6 PXE Boot support. If disabled, IPv6 PXE Boot Option is not supported.

IPv6 HTTP Support

Enable IPv6 HTTP Boot support. If disabled, IPv6 HTTP Boot Option is not supported.

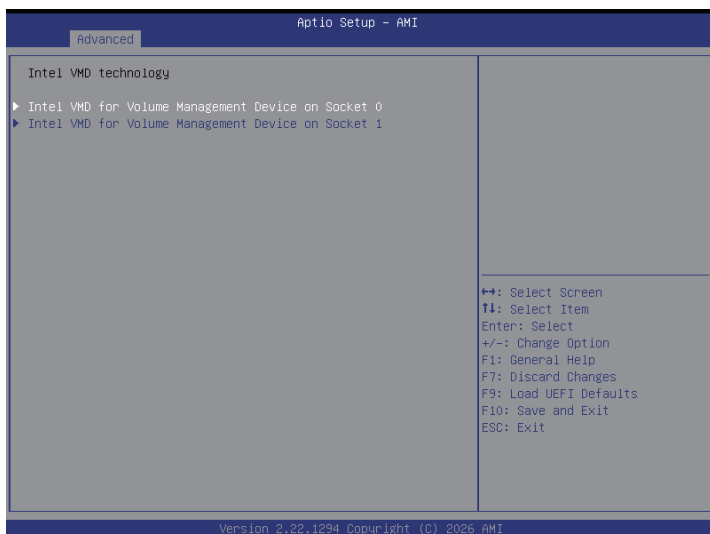
PXE Boot Wait Time

Specifies the wait time and press the ESC key to abort the PXE boot.

Media Detect Count

Specifies the number of times the presence of physical storage device are verified on a system reset or power cycle.

3.3.12 Intel VMD technology



Intel VMD for Volume Management Device on Socket 0/1

Use this item to enable or disable Intel Volume Management Device Technology in specific Stack.

VMD Config for Stack 0 (MCIO4/MCIO3), Stack1 (M2_2/M2_1), Stack2 (MCIO2/MCIO1), Stack3 (MCIO6/MCIO5), Stack4 (MCIO10/MCIO9), Stack5 (MCIO8/MCIO7)

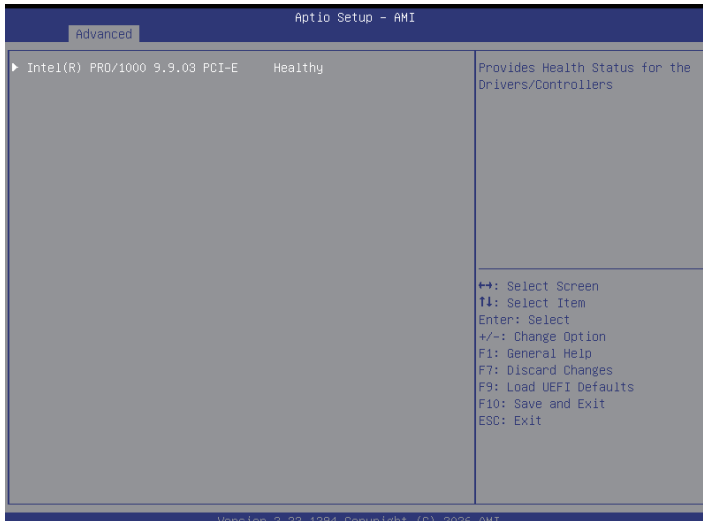
Use this item to enable or disable Intel Volume Management Device Technology in specific Stack.

When [Enabled], user is allowed to configure the items below.

VMD Port X

Use this item to enable or disable Intel Volume Management Device Technology on specific root port.

3.3.13 Driver Health

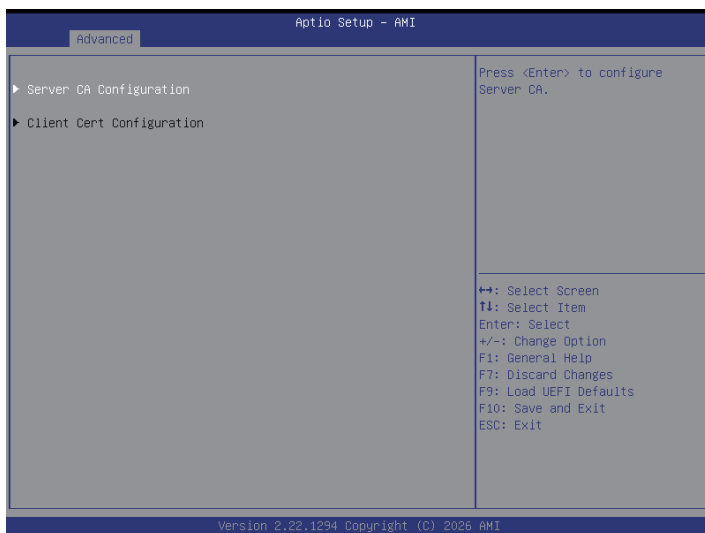


Inter (R) PRO/1000 9.9.03 PCI-E

Healthy

Provides Health Status for the Drivers and Controllers.

3.3.14 Tls Auth Configuration



Server CA Configuration

Press <Enter> to configure Server CA.

Client Cert Configuration

Press <Enter> to configure Client Cert.

Enroll Cert

Press <Enter> to enroll cert.

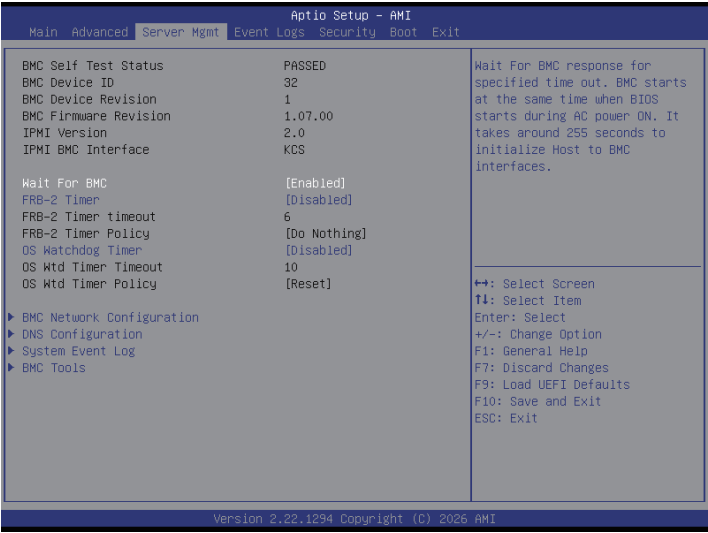
Delete Cert

Press <Enter> to delete cert.

3.3.15 Instant Flash

Instant Flash is a UEFI flash utility embedded in Flash ROM. This convenient UEFI update tool allows user to update system UEFI without entering operating systems first like MS-DOS or Windows[®]. Just save the new UEFI file to the USB flash drive, floppy disk or hard drive and launch this tool, then update the UEFI only in a few clicks without preparing an additional floppy diskette or other complicated flash utility. Please be noted that the USB flash drive or hard drive must use FAT32/16/12 file system. Execute the Instant Flash utility, the utility will show the UEFI files and the respective information. Select the proper UEFI file to update UEFI, and reboot the system after the UEFI update process is completed.

3.4 Server Mgmt



Wait For BMC

Wait For BMC response for specified time out. BMC starts at the same time when BIOS starts during AC power ON. It takes around 90 seconds to initialize Host to BMC interfaces.

FRB-2 Timer

Select this item to enable or disable FRB-2 timer (POST timer)

FRB-2 Timer Timeout

Select this item to define the FRB-2 Time Expiration between 1 to 30 value.

FRB-2 Timer Policy

Configure how the system should respond. If the FRB-2 Timer expires is disabled, this item is not available.

OS Watchdog Timer

Select this item to enable or disable OS Watchdog Timer. If enabled, starts a BIOS timer which can only be shut off by Management Software after the OS loads.

OS Wtd Timer Timeout

Configure the OS Boot Watchdog Timer Expiration between 1 to 30 min value. If the OS Boot Watchdog Timer is disabled, this item is not available.

OS Wtd Timer Policy

Configure how the system should respond if the OS Boot Watchdog Timer expires. If the OS Boot Watchdog Timer is disabled, this item is not available.

BMC Network Configuration

Select this item to configure BMC network parameters.

DNS Configuration

Select this item to configure DNS parameters.

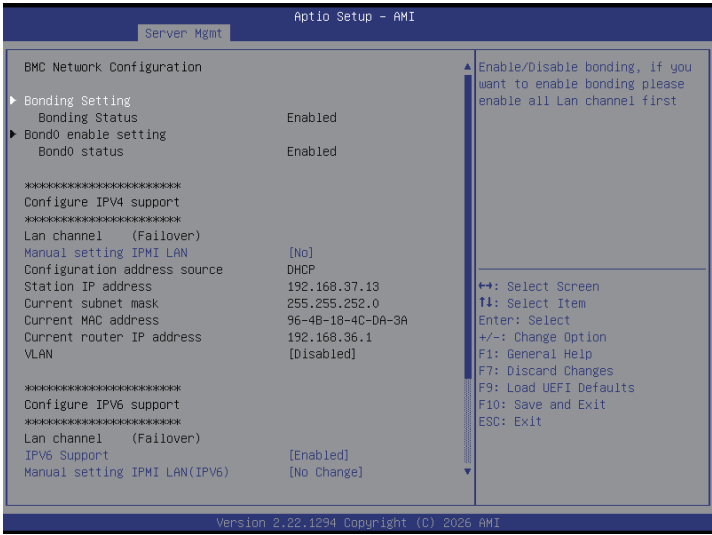
System Event Log

Press <Enter> to change the SEL event log configuration.

BMC Tools

Select this item to configure about KCS control, restore AC power loss and load BMC default settings.

3.4.1 BMC Network Configuration



Bonding Setting

Select this item to enabled or disabled bonding. Please enable all lan channel first when want to enable bonding.

Lan Channel (Failover)

Manual Setting IPMI LAN

If [No] is selected, the IP address is assigned by DHCP. Using a static IP address, toggle to [Yes], and the changes take effect after the system reboots. The default value is [No].

Configuration Address Source

Select to configure BMC network parameters statically or dynamically(by BIOS or BMC). Configuration options: [Static] and [DHCP].

Static: Manually enter the IP Address, Subnet Mask and Gateway Address in the BIOS for BMC LAN channel configuration.

DHCP: IP address, Subnet Mask and Gateway Address are automatically assigned by the network's DHCP server.



When [DHCP] or [Static] is selected, do NOT modify the BMC network settings on the IPMI web page.



The default login information for the IPMI web interface is:

Username: admin

Password: admin

For more instructions on how to set up remote control environment and use the IPMI management platform, please refer to the IPMI Configuration User Guide or go to the Support website at: <http://www.asrockrack.com/support/ipmi.asp>

VLAN

Enabled or disabled Virtual Local Area Network.

If [Enabled] is selected, configure the items below.

VLAN ID: Select this item to configure the VLAN ID setting, the Maximum value is 4094 and the Minimum value is 1.

VLAN Priority: Select this item to configure the VLAN Priority setting, the Maximum value is 7 and the Minimum value is 0.

IPV6 Support

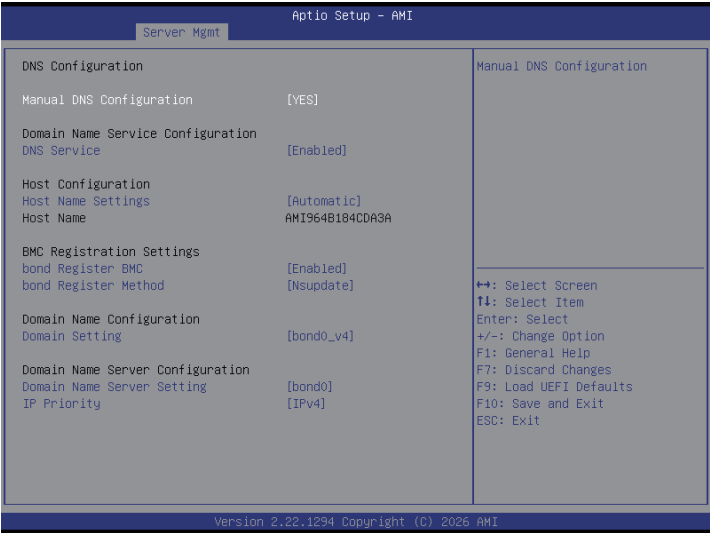
Enable or disable LAN1 IPV6 Support.

Manual Setting IPMI LAN(IPV6)

Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC).

Unspecified option will not modify any BMC network parameters during BIOS phase.

3.4.2 DNS Configuration



Manual DNS Configuration

Select this item to manual configure DNS.

If [YES] is selected, configure the items below.

DNS Service

Use this item to enable or disable DNS Service Configuration.

Host Name Settings

Use this item to automatic or manual Host Name Settings.

Bond Register BMC

Use this item to enable or disable Bond Register BMC.

Bond Register Method

Use this item to configure Bond Register Method with Nsupdate or DHCP client FQDN/Hostname..

Domain Setting

This item supports Manual, Bond0_v4 and Bond0_v6 Domain Settings.

Domain Name Server Setting

This item supports Manual and Bond0 DNS Server Settings.

IP Priority

This item supports IPV4 and IPV6 IP Priority.

3.4.3 System Event Log



SEL Components

Change this to enable or disable event logging for error/progress codes during boot.

Erase SEL

Use this to choose options for erasing SEL.

When SEL is Full

Use this to choose options for reactions to a full SEL.

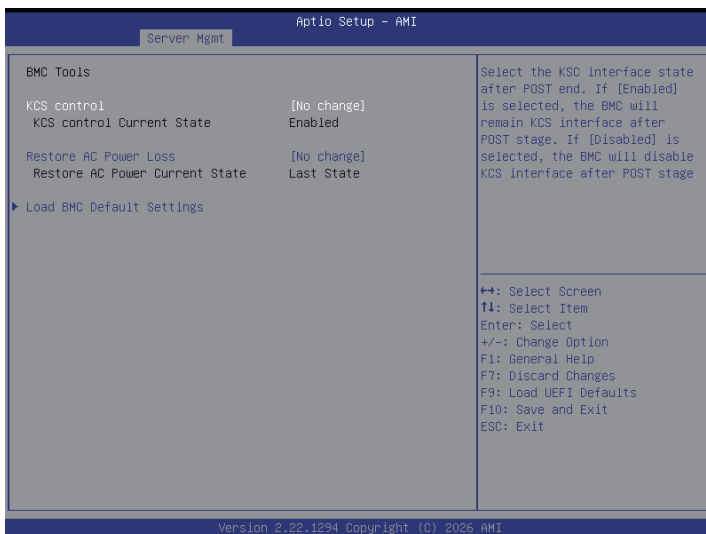
Log EFI Status Codes

Use this item to disable the logging of EFI Status Codes or log only error code or only progress code or both.

PCIe Device Degrade ELog Support

Use this item to enable or disable PCIe Device Degrade Error Logging Support.

3.4.4 BMC Tools



KCS control

Select the KSC interface state after POST end. If [Enabled] is selected, the BMC will remain KCS interface after POST stage. If [Disabled] is selected, the BMC will disable KCS interface after POST stage.

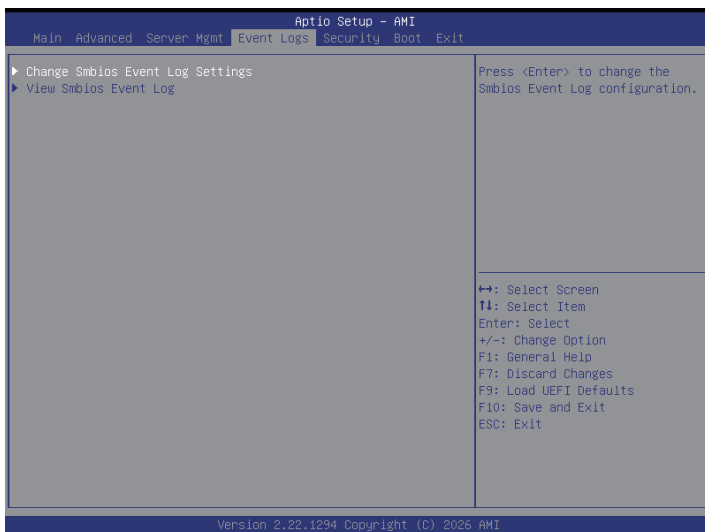
Restore AC Power Loss

This allows user to set the power state after an unexpected AC/power loss. If [Power Off] is selected, the AC/power remains off when the power recovers. If [Power On] is selected, the AC/power resumes and the system starts to boot up when the power recovers. If [Last State] is selected, it will recover to the state before AC/power loss.

Load BMC Default Settings

Use this item to load BMC default settings.

3.5 Event Logs



Change Smbios Event Log Settings

Select this item to configure the Smbios Event Log Settings.

When entering the item, the screen displays following sub-items:

Smbios Event Log

Use this item to enable or disable all features of the SMBIOS Event Logging during system boot.

Erase Event Log

The options include [No], [Yes, Next reset] and [Yes, Every reset]. If Yes is selected, all logged events will be erased.

When Log is Full

Use this item to choose options for reactions to a full Smbios Event Log. The options include [Do Nothing] and [Erase Immediately].

Log System Boot Event

Choose option to enable or disable logging of System boot event.

View Smbios Event Log

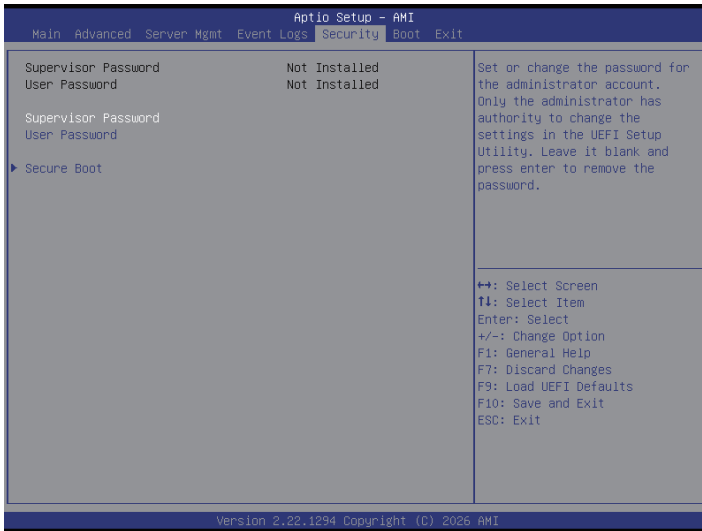
Press <Enter> to view the Smbios Event Log records.



All values changed here do not take effect until computer is restarted.

3.6 Security

This section allows user to set or change the supervisor/user password for the system. For the user password item is allowed user to clear it.



Supervisor Password

Set or change the password for the administrator account. Only the administrator has authority to change the settings in the UEFI Setup Utility. Leave it blank and press enter to remove the password.

User Password

Set or change the password for the user account. Users are unable to change the settings in the UEFI Setup Utility. Leave it blank and press enter to remove the password.

Secure Boot

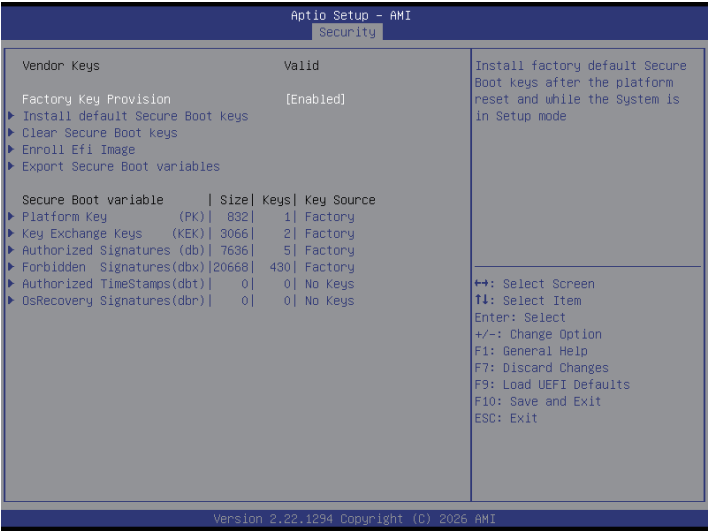
Use this to enable or disable Secure Boot Control. The default value is [Disabled]. Enable to support Windows Server 2012 R2 or later versions Secure Boot.

Secure Boot Mode

Secure Boot mode selector: Standard/Custom. In Custom mode Secure Boot Variables can be configured without authentication.

3.6.1 Expert Key Management

In this section, expert users can modify Secure Boot Policy variables without full authentication.



Factory Key Provision

Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode.

Install Default Secure Boot Keys

Please install default secure boot keys if it's the first time using the secure boot.

Clear Secure Boot Keys

Force System to Setup Mode - clear all Secure Boot Variables. Change takes effect after re-boot.

Enroll Efi Image

Allow the image to run in Secure Boot mode. Enroll SHA256 hash of the binary into Authorized Signature Database (db).

Export Secure Boot Variables

Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device.

Platform Key(PK)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

- a) EFI_SIGNATURE_LIST
- b) EFI_CERT_X509 (DER)
- c) EFI_CERT_RSA2048 (bin)
- d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

Key Exchange Keys(KEK)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

- a) EFI_SIGNATURE_LIST
- b) EFI_CERT_X509 (DER)
- c) EFI_CERT_RSA2048 (bin)
- d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

Authorized Signatures(db)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

- a) EFI_SIGNATURE_LIST
- b) EFI_CERT_X509 (DER)
- c) EFI_CERT_RSA2048 (bin)
- d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

Forbidden Signatures(dbx)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

Authorized TimeStamps(dbt)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

OsRecovery Signatures(dbr)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

3.7 Boot Screen

In this section, it displays the available devices on the system and allows user to configure the boot settings and the boot priority.



Boot Option #1/#2/#3/#4/#5/#6

Use this item to set the system boot order.

UEFI USB Drive BBS Priorities

Specify the Boot Device Priority sequence from available UEFI USB Drives.

UEFI Application Boot Priorities

Specify the Boot Device Priority sequence from available UEFI Application.

Setup Prompt Timeout

Configure the number of seconds to wait for the UEFI setup utility.

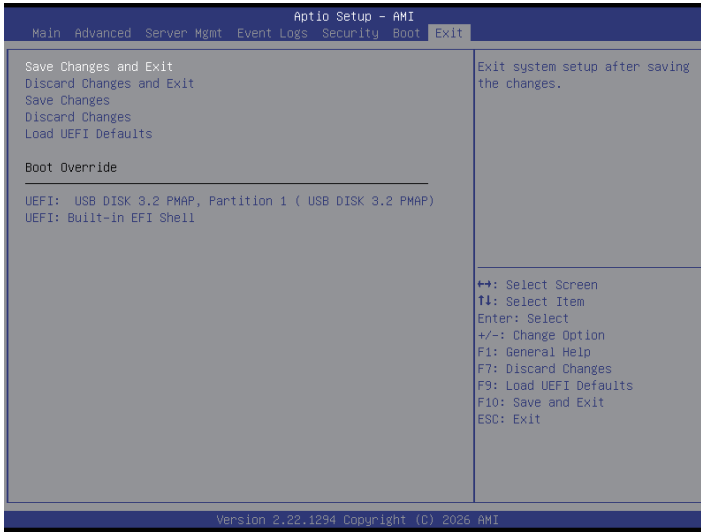
Bootup NumLock State

If this item is set to [On], it will automatically activate the Numeric Lock function after boot-up.

Full Screen Logo

Use this item to enable or disable OEM Logo. The default value is [Enabled].

3.8 Exit Screen



Save Changes and Exit

When selecting this option, the following message “Save configuration changes and exit setup?” will pop-out. Press <F10> key or select [Yes] to save the changes and exit the UEFI SETUP UTILITY.

Discard Changes and Exit

When selecting this option, the following message “Discard changes and exit setup?” will pop-out. Press <ESC> key or select [Yes] to exit the UEFI SETUP UTILITY without saving any changes.

Save Changes

When selecting this option, the following message “Save changes?” will pop-out. Press <F7> key or select [Yes] to save all changes.

Discard Changes

When selecting this option, the following message “Discard changes?” will pop-out. Press <F7> key or select [Yes] to discard all changes.

Load UEFI Defaults

Load UEFI default values for all the setup questions. F9 key can be used for this operation.

Chapter 4 Software Support

After all the hardware has been installed, it suggests to go to the official website at <http://www.ASRockRack.com> and make sure if there are any new updates of the BIOS / BMC firmware for the motherboard.

4.1 Download and Install Operating System

This motherboard supports various Microsoft® Windows® Server / Linux compliant operating systems. Please download the operating system from the OS manufacturer. Please refer to the OS documentation for more instructions.

**Please download the Intel® Rapid Storage Technology driver from the ASRock Rack's website (www.asrockrack.com) to the USB drive while installing OS in SATA RAID mode.*

4.2 Download and Install Software Drivers

This motherboard supports various Microsoft® Windows® compliant drivers. Please download the required drivers from the website at <http://www.ASRockRack.com>.

To download necessary drivers, go to the product page, click on the "Download" tab, choose the operating system that is used, and then download the using driver.

Chapter 5 Troubleshooting

5.1 Troubleshooting Procedures

Follow the procedures below to troubleshoot the system.



Always unplug the power cord before adding, removing or changing any hardware components. Failure to do so may cause physical injuries and damages to motherboard components.

1. Disconnect the power cable and check whether the PWR LED is off.
2. Unplug all cables, connectors and remove all add-on cards from the motherboard.
Make sure that the jumpers are set to default settings.
3. Confirm that there are no short circuits between the motherboard and the chassis.
4. Install a CPU and fan on the motherboard, then connect the chassis speaker and power LED.

If there is no power...

1. Confirm that there are no short circuits between the motherboard and the chassis.
2. Make sure that the jumpers are set to default settings.
3. Check the settings of the 115V/230V switch on the power supply.
4. Verify if the battery on the motherboard provides ~3VDC. Install a new battery if it does not.

If there is no video...

1. Try replugging the monitor cables and power cord.
2. Check for memory errors.

If there are memory errors...

1. Verify that the DIMM modules are properly seated in the slots.
2. Use recommended DDR5 RDIMM/RDIMM-3DS/MRDIMM.
3. Install more than one DIMM modules that should be identical with the same brand, speed, size and chip-type.
4. Try inserting different DIMM modules into different slots to identify faulty ones.
5. Check the settings of the 115V/230V switch on the power supply.

Unable to save system setup configurations...

1. Verify if the battery on the motherboard provides ~3VDC. Install a new battery if it does not.
2. Confirm whether the power supply provides adequate and stable power.

Other problems...

1. Try searching keywords related to the related problem on ASRock Rack's FAQ page:
<http://www.asrockrack.com/support>

5.2 Technical Support Procedures

If the problems are still unsolved, please contact ASRock Rack's technical support with the following information:

1. Contact information
2. Model name, BIOS version and problem type.
3. System configuration.
4. Problem description.

Contact ASRock Rack's technical support at:
<http://www.asrockrack.com/support/tsd.asp>

5.3 Returning Merchandise for Service

For warranty service, the receipt or a copy of the invoice marked with the date of purchase is required. By calling the vendor or going to RMA website (<http://event.asrockrack.com/tsd.asp>) to obtain a Returned Merchandise Authorization (RMA) number.

The RMA number should be displayed on the outside of the shipping carton which is mailed prepaid or hand-carried when returning the motherboard to the manufacturer. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty does not cover damages incurred in shipping or from failure due to alteration, misuse, abuse or improper maintenance of products.

Contact the distributor first for any product related problems during the warranty period.

Contact Information

If it needs to contact ASRock Rack or want to know more about ASRock Rack, you're welcome to visit ASRock Rack's website at <http://www.asrockrack.com>; or contact the dealer for further information. For technical questions, please submit a support request form at <https://event.asrockrack.com/tsd.asp>

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