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Server/Workstation
Motherboard

GNR2D32G-2L+

User Manual

English



Version 1.31

Published Jan. 2026

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- (1) this device may not cause harmful interference, and
- (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.



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ASRock Rack INC. hereby declares that this device is in compliance with the essential requirements and other relevant provisions of related UKCA Directives. Full text of UKCA declaration of conformity is available at: <http://www.asrockrack.com>



DO NOT throw the motherboard in municipal waste. This product has been designed to enable proper reuse of parts and recycling. This symbol of the crossed out wheeled bin indicates that the product (electrical and electronic equipment) should not be placed in municipal waste. Check local regulations for disposal of electronic products.

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Chapter 1 Introduction

Thank you for purchasing ASRock Rack **GNR2D32G-2L+** motherboard, a reliable motherboard produced under ASRock Rack's consistently stringent quality control. It delivers excellent performance with robust design conforming to ASRock Rack's commitment to quality and endurance.

In this manual, chapter 1 and 2 contains introduction of the motherboard and step-by-step guide to the hardware installation. Chapter 3 and 4 contains the configuration guide to BIOS setup and information of the software support.



Because the motherboard specifications and the BIOS software might be updated, the content of this manual will be subject to change without notice. In case any modifications of this manual occur, the updated version will be available on ASRock Rack website without further notice. Find the latest memory and CPU support lists on ASRock Rack website as well. ASRock Rack's Website: www.ASRockRack.com

*Please visit the website for specific information and technical support:
<http://www.asrockrack.com/support/>*

1.1 Package Contents

- ASRock Rack GNR2D32G-2L+ motherboard
(Proprietary form factor: 16.93" x 13.79", 43cm x 35cm)
- Quick installation guide
- 4 CPU Non-Fabric carriers (2xE2A, 2xE2B)
- 1 ATX 4P to 24P power cable
- 1 Screw for M.2 socket



If any items are missing or appear damaged, contact the authorized dealer.

1.2 Specifications

GNR2D32G-2L+	
Physical Status	
Form Factor	Proprietary
Dimension	16.93" x 13.79" (43cm x 35cm)
Processor System	
CPU	Supports Intel® Xeon® 6700P-series, 6500P-series, and 6700E-series processors
Socket	1+1 Socket E2 (LGA4710)
Chipset	System on Chip
System Memory	
Supported DIMM Quantity	16+16 DIMM slots (2DPC)
Supported Type	DDR5 RDIMM DDR5 MRDIMM (1DPC only)
Max. Capacity per DIMM	RDIMM: 128GB MRDIMM: 64GB
Max. Frequency	RDIMM: 6400MT/s (1DPC), 6000MT/s (2DPC) MRDIMM: 8000MT/s (1DPC only)
Voltage	1.1V
<i>Note: Memory support is to be validated.</i>	
Other PCIe Expansion Connectors	
M.2	1 M-key (PCIe5.0 x4), supports 22110/2280 form factor [CPU0]
MCIO	10 MCIO (PCIe5.0/CXL2.0 x8) [CPU0] 10 MCIO (PCIe5.0/CXL2.0 x8) [CPU1] 1 MCIO (PCIe5.0 x8) [CPU1]
Ethernet	
Additional GbE Controller	2 RJ45 (1GbE) by Intel® i350
Server Management	
BMC Controller	ASPEED AST2600: IPMI2.0 with iKVM and vMedia support
IPMI Dedicated GLAN	1 Realtek RTL8211F for dedicated management GLAN
Graphics	
Controller	ASPEED AST2600: 1 DB15 (VGA), 1(15-pin) header
Rear I/O	
UID Button/LED	1 UID button w/ LED
Other Buttons/LEDs	1 PWR button, 1 RST button, 1 NMI button, 1 HDD LED, 1 SYS LED
Video Output	1 DB15 (VGA)

USB Port	4 Type-A (USB3.2 Gen1)
LAN Port	2 RJ45 (1GbE), 1 dedicated IPMI
Internal Connectors/Headers	
Power Connector	6 Micro-hi (8-pin, ATX 12V), 1 Micro-Fit (4-pin, ATX PSU signal) w/ ATX 24-pin adapter cable, 1 Micro-Fit (2-pin, 5V)
Auxiliary Panel Header	1 (18-pin): chassis intrusion, system fault LED, LAN1/LAN2 activity LED, locate, SMBus
System Panel Header	1 (9-pin): power switch, reset switch, system power LED, HDD activity LED
NMI Header	1
COM Header	1 (9-pin)
VGA Header	1
Fan Header	6 (6-pin)
TPM Header	1 (13-pin, SPI)
VROC Header	1
HSBP	2
SMBus Headers	3
PMBus Header	1
IPMB Header	1
Clear CMOS	1 (contact pads)
USB Header	1 (19-pin, 2 USB3.2 Gen1)
Others	1 NCSI header, 1 LCM header, 1 RL LED header, 1 IPMI LED header
LED Indicators	
Standby Power LED	1 (5VSB)
80 Debug Port LED	1
Fan Fail LED	6
BMC Heartbeat LED	1
Other LEDs	1 CPLD Heartbeat LED, 1 System Caterr LED
System BIOS	
Type	AMI UEFI BIOS; 512Mb SPI Flash ROM
Features	Plug and Play, ACPI 4.0 and above compliance wake up events, SMBIOS 3.4 and above, ASRock Rack Instant Flash
Hardware Monitor	
Temperature	CPU, MB, Card side Temperature Sensing
Fan	Fan Tachometer CPU Quiet Fan (Allow Chassis Fan Speed Auto-Adjust by CPU Temperature) Fan Multi-Speed Control

Voltage	P0_VDDCR_CPU0, P0_VDDCR_CPU1, P0_VDDCR_SOC, P0_VDD_18_DUAL, P0_VDD_11_S3, P0_VDDIO, P1_VDDCR_CPU0, P1_VDDCR_CPU1, P1_VDDCR_SOC, P1_VDD_18_DUAL, P1_VDD_11_S3, P1_VDDIO, +BAT, +12V, +3VSB, +5VSB
Support OS	
OS	Microsoft® Windows® - Server 2022 (64bit) - Server 2025 (64bit) Linux® - Red Hat Enterprise Linux Server 9.4 (64bit) - SUSE Enterprise Linux Server 15 SP6 (64bit) - Ubuntu 24.04 (64bit) <i>*Please refer to the website for the latest OS support list.</i>
Environment	
Temperature	Operation Temperature: 10°C ~ 35°C Non Operation Temperature: -40°C ~ 70°C
Humidity	Non operation humidity: 20% ~ 90% (Non condensing)

NOTE: Please refer to the website for the latest specifications.



This motherboard supports Wake from on Board LAN. To use this function, please make sure that the "Wake on Magic Packet from power off state" is enabled in Device Manager > Intel® Ethernet Connection > Power Management. And the "PCI Devices Power On" is enabled in UEFI SETUP UTILITY > Advanced > ACPI Configuration. After that, onboard LAN1&2 can wake up S5 under OS.

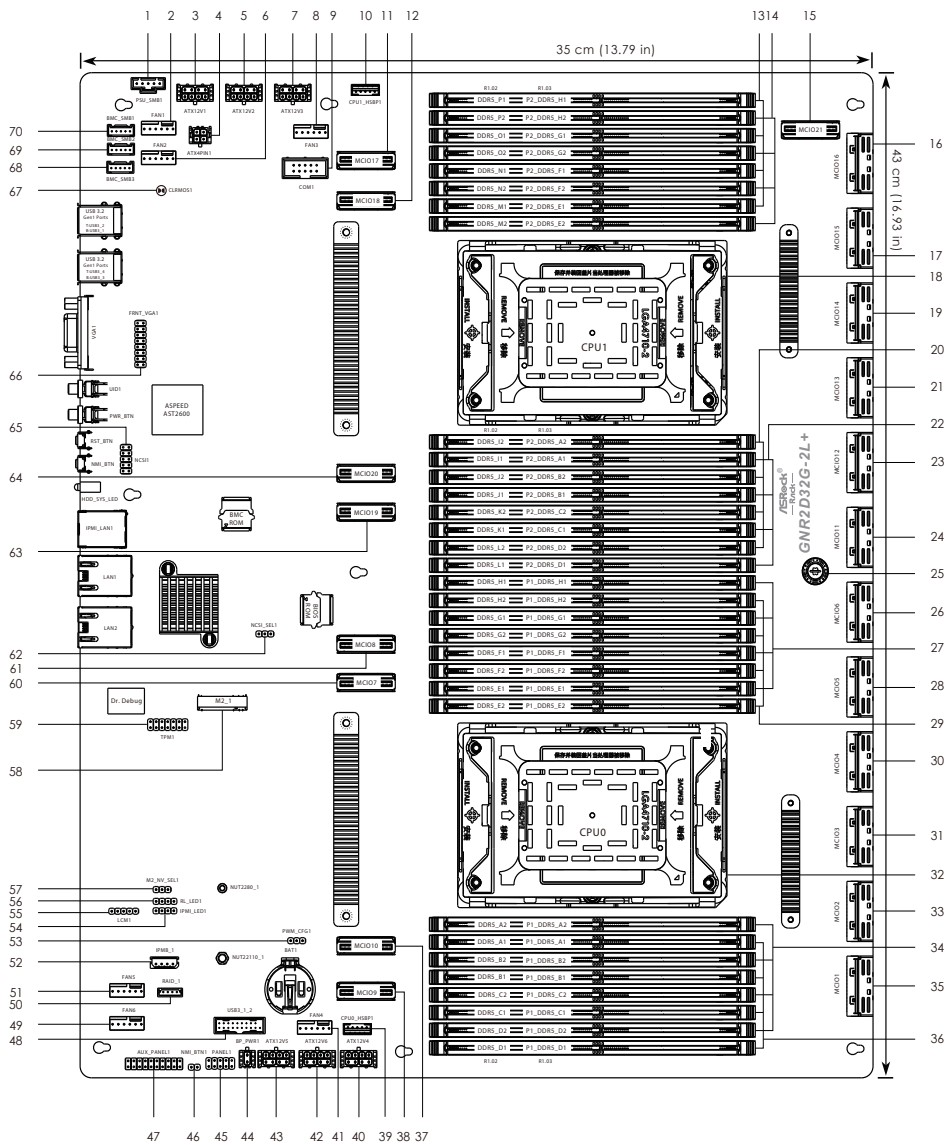


If installing Intel® LAN utility or Marvell SATA utility, this motherboard may fail Windows® Hardware Quality Lab (WHQL) certification tests. If installing the drivers only, it will pass the WHQL tests.

1.3 Unique Features

ASRock Rack Instant Flash is a BIOS flash utility embedded in Flash ROM. This convenient BIOS update tool allows user to update system BIOS without entering operating systems first like MS-DOS or Windows*. With this utility, press the <F6> key during the POST or the <F2> key to enter into the BIOS setup menu to access ASRock Rack Instant Flash. Just launch this tool and save the new BIOS file to the USB flash drive, floppy disk or hard drive, then update the BIOS only in a few clicks without preparing an additional floppy diskette or other complicated flash utility. Please be noted that the USB flash drive or hard drive must use FAT32/16/12 file system.

1.4 Motherboard Layout



The illustration here is for references only. The actual layout may slightly vary depending on the model and the version used.

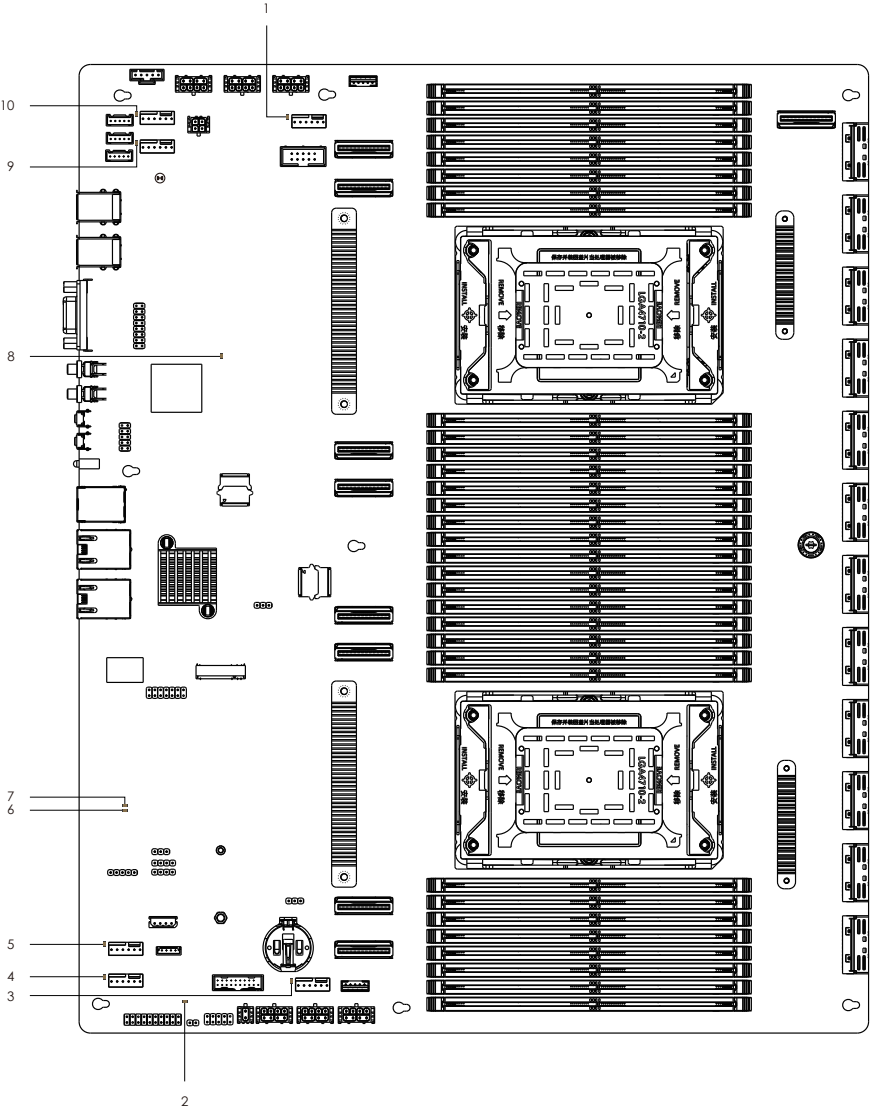
No.	Description
1	PSU SMBus (PSU_SMB1)
2	System Fan Header (FAN1)
3	ATX 12V Power Connector (ATX12V1)
4	Micro-Fit Power Connector (ATX4PIN1)
5	ATX 12V Power Connector (ATX12V2)
6	System Fan Header (FAN2)
7	ATX 12V Power Connector (ATX12V3)
8	System Fan Header (FAN3)
9	COM Port Header (COM1)
10	Backplane PCI Express Hot-Plug Connector (CPU1_HSBP1)
11	Mini Cool Edge IO Connector (MCIO17)
12	Mini Cool Edge IO Connector (MCIO18)
13	R1.02: 4 DDR5 DIMM Slots (DDR5_M1/N1/O1/P1)*
	R1.03: 4 DDR5 DIMM Slots (P2_DDR5_E1/F1/G1/H1)*
14	R1.02: 4 DDR5 DIMM Slots (DDR5_M2/N2/O2/P2)*
	R1.03: 4 DDR5 DIMM Slots (P2_DDR5_E2/F2/G2/H2)*
15	Mini Cool Edge IO Connector (MCIO21)
16	Mini Cool Edge IO Connector (MCIO16)
17	Mini Cool Edge IO Connector (MCIO15)
18	Socket E2 (LGA4710) (CPU1)
19	Mini Cool Edge IO Connector (MCIO14)
20	R1.02: 4 DDR5 DIMM Slots (DDR5_I2/J2/K2/L2)*
	R1.03: 4 DDR5 DIMM Slots (P2_DDR5_A2/B2/C2/D2)*
21	Mini Cool Edge IO Connector (MCIO13)
22	R1.02: 4 DDR5 DIMM Slots (DDR5_I1/J1/K1/L1)*
	R1.03: 4 DDR5 DIMM Slots (P2_DDR5_A1/B1/C1/D1)*
23	Mini Cool Edge IO Connector (MCIO12)
24	Mini Cool Edge IO Connector (MCIO11)
25	Thumbscrew
26	Mini Cool Edge IO Connector (MCIO6)
27	R1.02: 4 DDR5 DIMM Slots (DDR5_E1/F1/G1/H1)*
	R1.03: 4 DDR5 DIMM Slots (P1_DDR5_E1/F1/G1/H1)*
28	Mini Cool Edge IO Connector (MCIO5)
29	R1.02: 4 DDR5 DIMM Slots (DDR5_E2/F2/G2/H2)*
	R1.03: 4 DDR5 DIMM Slots (P1_DDR5_E2/F2/G2/H2)*
30	Mini Cool Edge IO Connector (MCIO4)

No.	Description
31	Mini Cool Edge IO Connector (MCIO3)
32	Socket E2 (LGA4710) (CPU0)
33	Mini Cool Edge IO Connector (MCIO2)
34	R1.02: 4 DDR5 DIMM Slots (DDR5_A2/B2/C2/D2)* R1.03: 4 DDR5 DIMM Slots (P1_DDR5_A2/B2/C2/D2)*
35	Mini Cool Edge IO Connector (MCIO1)
36	R1.02: 4 DDR5 DIMM Slots (DDR5_A1/B1/C1/D1)* R1.03: 4 DDR5 DIMM Slots (P1_DDR5_A1/B1/C1/D1)*
37	Mini Cool Edge IO Connector (MCIO10)
38	Mini Cool Edge IO Connector (MCIO9)
39	Backplane PCI Express Hot-Plug Connector (CPU0_HSBP1)
40	ATX 12V Power Connector (ATX12V4)
41	System Fan Header (FAN4)
42	ATX 12V Power Connector (ATX12V6)
43	ATX 12V Power Connector (ATX12V5)
44	HDD Backplane Power Connector (BP_PWR1)
45	System Panel Header (PANEL1)
46	Non Maskable Interrupt Button (NMI_BTN1)
47	Auxiliary Panel Header (AUX_PANEL1)
48	USB 3.2 Gen1 Header (USB3_1_2)
49	System Fan Header (FAN6)
50	Virtual RAID On CPU Header (RAID_1)
51	System Fan Header (FAN5)
52	Intelligent Platform Management Bus Header (IPMB_1)
53	PWM Configuration Header (PWM_CFG1)
54	IPMI LAN LED Header (IPMI_LED1)
55	Liquid Crystal Module Header (LCM1)
56	Rear Panel LAN LED (RL_LED1)
57	M.2 Signal Source Selection Jumper (M2_NV_SEL1)
58	M.2 Socket (M2_1) (Type 22110 / 2280)
59	SPI TPM Header (TPM1)
60	Mini Cool Edge IO Connector (MCIO7)
61	Mini Cool Edge IO Connector (MCIO8)
62	NCSI Mode Jumper (NCSI_SEL1)

No.	Description
63	Mini Cool Edge IO Connector (MCIO19)
64	Mini Cool Edge IO Connector (MCIO20)
65	Network Controller Sideband Interface Header (NCSI1)
66	Front VGA Header (FRNT_VGA1)
67	Clear CMOS Pad (CLRMOS1)
68	BMC SMBus Header (BMC_SMB3)
69	BMC SMBus Header (BMC_SMB2)
70	BMC SMBus Header (BMC_SMB1)

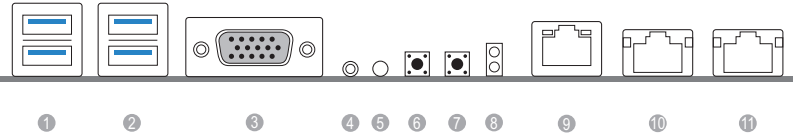
**For DIMM installation and configuration instructions, please see p.22 (Installation of Memory Modules (DIMM)) for more details.*

1.5 Onboard LED Indicators



No.	Item	Status	Description
1	FAN_LED3	Red	FAN3 failed
2	SB_PWR1	Green	STB PWR ready
3	FAN_LED4	Red	FAN4 failed
4	FAN_LED6	Red	FAN6 failed
5	FAN_LED5	Red	FAN5 failed
6	LED_CPLD_HB1	Green	CPLD heartbeat LED
7	LED_CATERR1	Red	CPU CATERR failed
8	BMC_LED1	Blinking four times and then off	Start initialization after AC power-on or BMC reset
		Blinking at 1Hz	BMC ready
		Steady on	Error
		Steady off Other frequency	(The actual behavior depends on the state at the time of failure)
9	FAN_LED2	Red	FAN2 failed
10	FAN_LED1	Red	FAN1 failed

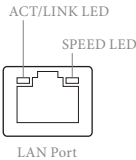
1.6 I/O Panel



No. Description		No. Description	
1	USB 3.2 Gen1 Ports (USB3_1_2)	7	NMI Button (NMI_BTN)
2	USB 3.2 Gen1 Ports (USB3_3_4)	8	HDD/System Fault LED (HDD_SYS_LED)
3	VGA Header (VGA1)	9	IPMI LAN Header (IPMI_LAN1)*
4	UID Switch (UID1)	10	1G LAN RJ-45 Port (LAN1, shared NIC)**
5	Power Switch/LED (PWR_BTN)	11	1G LAN RJ-45 Port (LAN2)**
6	Reset Button (RST_BTN)		

LAN Port LED Indications

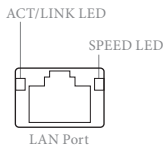
*There is an LED on each side of IPMI LAN port. Please refer to the table below for the LAN port LED indications.



IPMI LAN Port LED Indications

Activity / Link LED		Speed LED	
Status	Description	Status	Description
Off	No link	Off	10Mbps connection or no link
Blinking Yellow	Data activity	Orange	100Mbps connection
On	Link	Green	1Gbps connection

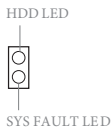
**There is an LED on each side of 1G LAN port. Please refer to the table below for the LAN port LED indications.



1G LAN Port (LAN1, LAN2) LED Indications

Activity / Link LED		Speed LED	
Status	Description	Status	Description
Off	No link	Off	10Mbps connection or no link
Blinking Yellow	Data activity	Orange	100Mbps connection
On	Link	Green	1Gbps connection

HDD/System Fault LED Indications



HDD LED		SYS FAULT LED	
Status	Description	Status	Description
Off	HDD inactive	Off	Normal
Green	HDD active	RED	System fault

The diagram illustrates a complex system architecture centered around two Intel GNR-SP CPUs (P0 and P1). Each CPU is connected to a set of DDR5 memory modules (R1.02 and R1.03). The system includes various peripheral connections such as USB 2.0, USB 3.0, LAN, and fan headers. A central USB 10/20/30 hub manages the data flow between the CPUs and the external devices. The diagram is color-coded: green for USB 2.0, blue for USB 3.0, and orange for LAN. The components are arranged in a symmetrical layout around the central hub and processors.

Chapter 2 Installation

This is a proprietary form factor (12" x 13", 30.5cm x 33cm) motherboard. Before installing the motherboard, study the configuration of the chassis to ensure that the motherboard fits into it.



1. Ensure the motherboard battery is installed before unplugging the power cord or installing/removing the motherboard.
2. Before installing or removing any component, ensure that the power is switched off or the power cord is detached from the power supply. Failure to do so may cause severe damage to the motherboard, peripherals, and/or components.

2.1 Screw Holes

Place screws into the holes indicated by circles to secure the motherboard to the chassis.



Do not over-tighten the screws! Doing so may damage the motherboard.

2.2 Pre-installation Precautions

Take note of the following precautions before installing motherboard components or change any motherboard settings.

1. Unplug the power cord from the wall socket before touching any components.
2. To avoid damaging the motherboard's components due to static electricity, NEVER place the motherboard directly on the carpet or the like. Also remember to use a grounded wrist strap or touch a safety grounded object before handling the components.
3. Hold components by the edges and do not touch the ICs.
4. Whenever uninstall any component, place it on a grounded anti-static pad or in the bag that comes with the component.
5. When placing screws into the screw holes to secure the motherboard to the chassis, please do not over-tighten the screws! Doing so may damage the motherboard.

2.3 Installing the CPU and Heatsink

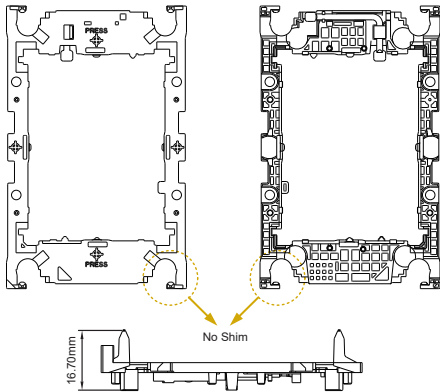


1. Unplug all power cables before installing the CPU.
2. Illustration in this documentation are examples only.

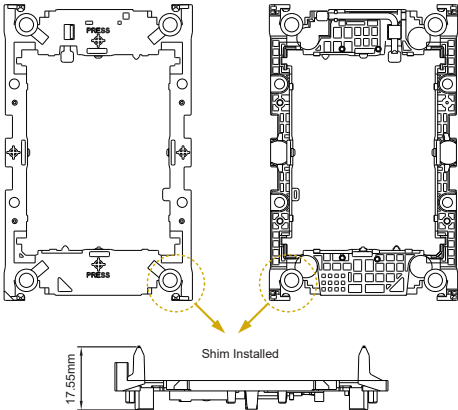
Carrier Used

Carrier Type	Xeon® SP XCC	Xeon® SP HCC/LCC/HDCC
Carrier Code	E2A	E2B
Shim	No	Yes
Carrier Height	16.70mm	17.55mm

XCC Carrier



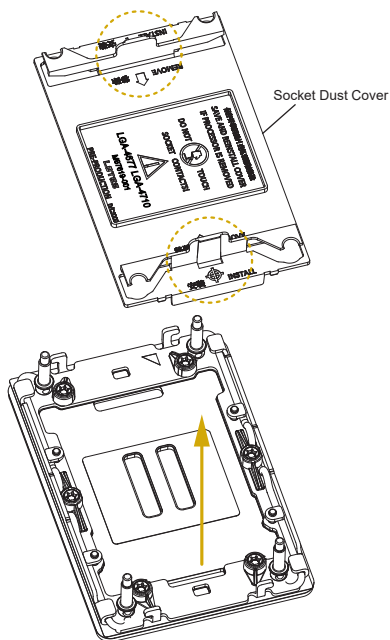
HCC/LCC/HDCC Carrier





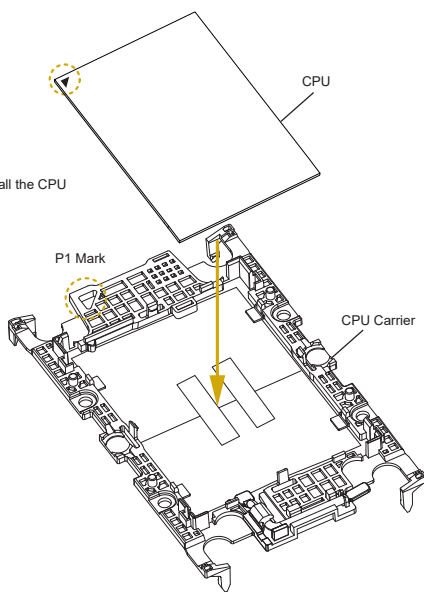
Before inserting the CPU into the socket, please check if the PnP cap is on the socket, if the CPU surface is unclean, or if there are any bent pins in the socket. Do not force to insert the CPU into the socket if above situation is found. Otherwise, the CPU will be seriously damaged.

1

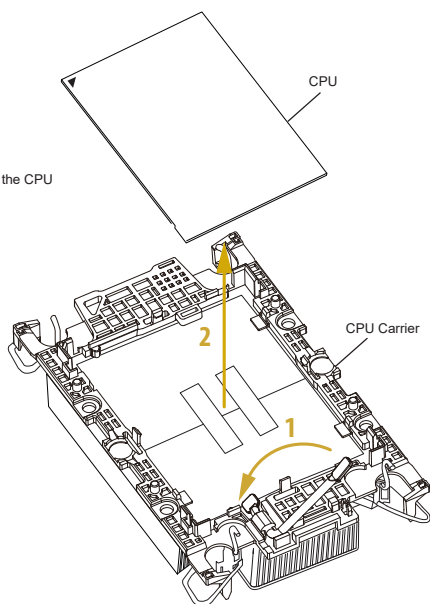


2

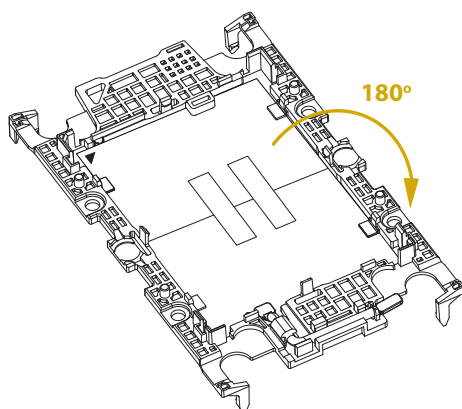
Installing CPU:
Align the Pin1 mark to install the CPU



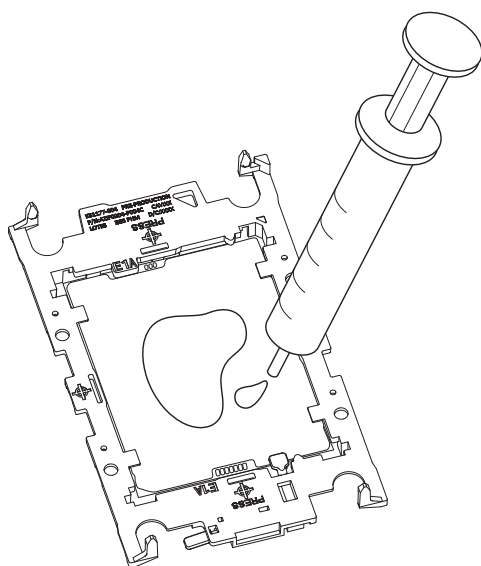
Removing CPU:
Press the lever to remove the CPU



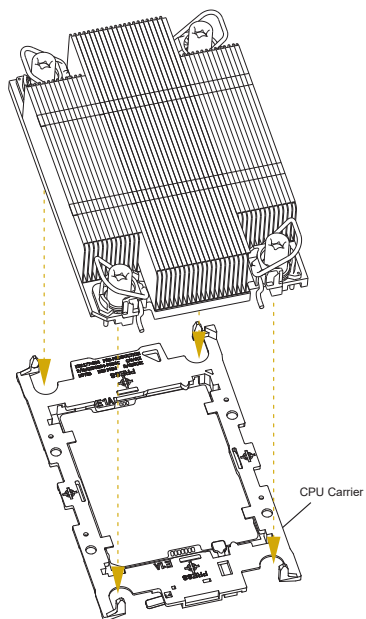
3



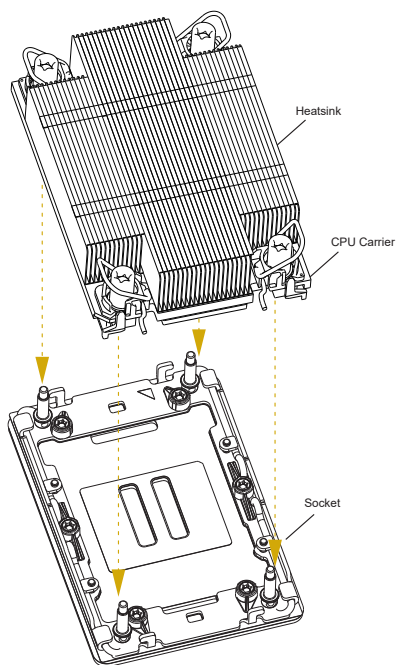
4



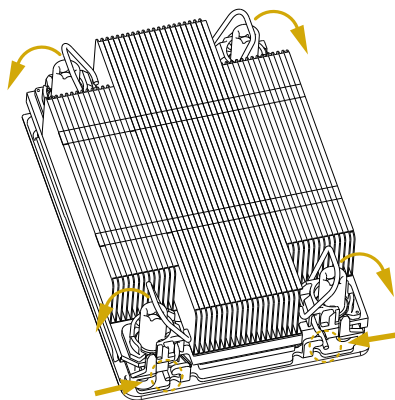
5



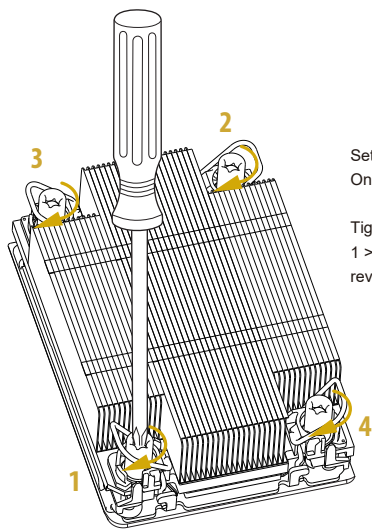
6



7



8



Set the torque wrench to 6-12 in-lb.
One fourth a turn each time.

Tighten the screws in a sequential order
1 > 2 > 3 > 4. Loosen the screws in a
reverse order.

2.4 Installation of Memory Modules (DIMM)

This motherboard provides thirty-two DDR5 (Double Data Rate 5) DIMM slots in two groups, and supports Dual Channel Memory Technology.

CPU0	CPU1
R1.02: DDR5_A1/B1/C1/D1/E1/F1/G1/H1 DDR5_A2/B2/C2/D2/E2/F2/G2/H2	R1.02: DDR5_I1/J1/K1/L1/M1/N1/O1/P1 DDR5_I2/J2/K2/L2/M2/N2/O2/P2
R1.03: P1_DDR5_A1/B1/C1/D1/E1/F1/G1/H1 P1_DDR5_A2/B2/C2/D2/E2/F2/G2/H2	R1.03: P2_DDR5_A1/B1/C1/D1/E1/F1/G1/H1 P2_DDR5_A2/B2/C2/D2/E2/F2/G2/H2



1. It is not allowed to install a DDR, DDR2, DDR3 or DDR4 memory module into a DDR5 slot; otherwise, this motherboard and DIMM may be damaged.
2. For dual channel configuration, it always needs to install identical (the same brand, speed, size and chip-type) DDR5 DIMM pairs.
3. It is unable to activate Dual Channel Memory Technology with only one or three memory module installed.

2.4.1 DIMM Population for DDR5

1 CPU Configurations

DIMM Slot		DIMM Number					
		1	2	4	6	8	16
CPU0	A1	V	V	V	V	V	V
	A2						V
	B1				V	V	V
	B2						V
	C1		V	V	V	V	V
	C2						V
	D1					V	V
	D2						V
	E1			V	V	V	V
	E2						V
	F1				V	V	V
	F2						V
	G1			V	V	V	V
	G2						V
	H1					V	V
	H2						V

The symbol V indicates the slot is populated.

2 CPU Configurations

DIMM Slot		DIMM Number					
		1	2	4	8	16	32
CPU0	A1	V	V	V	V	V	V
	A2						V
	B1					V	V
	B2						V
	C1			V	V	V	V
	C2						V
	D1					V	V
	D2						V
	E1				V	V	V
	E2						V
	F1					V	V
	F2						V
	G1				V	V	V
	G2						V
	H1					V	V
	H2						V

DIMM Slot			DIMM Number					
	R1.02	R1.03	1	2	4	6	16	32
CPU1	I1	A1		V	V	V	V	V
	I2	A2						V
	J1	B1					V	V
	J2	B2						V
	K1	C1			V	V	V	V
	K2	C2						V
	L1	D1					V	V
	L2	D2						V
	M1	E1				V	V	V
	M2	E2						V
	N1	F1					V	V
	N2	F2						V
	O1	G1				V	V	V
	O2	G2						V
	P1	H1					V	V
	P2	H2						V

The symbol V indicates the slot is populated.

2.4.2 DIMM Population for DDR5 and CPS

1 CPU Configuration (DDR5+CPS)

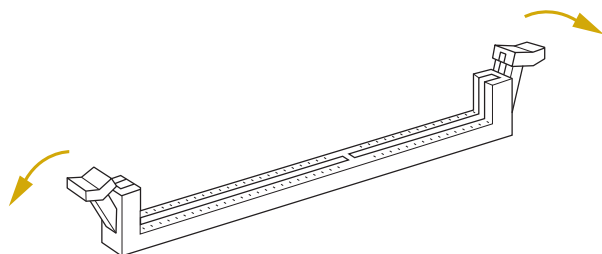
CPU0						
DDR5 + CPS	4 DDR5 + 4 CPS	6 DDR5 + 1 CPS	8 DDR5 + 1 CPS	8 DDR5 + 4 CPS	8 DDR5 + 4 CPS	8 DDR5 + 8 CPS
A1	CPS	DDR5	DDR5	DDR5	DDR5	DDR5
A2				CPS		CPS
B1	DDR5	CPS	DDR5	DDR5	DDR5	DDR5
B2					CPS	CPS
C1	CPS	DDR5	DDR5	DDR5	DDR5	DDR5
C2				CPS		CPS
D1	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5
D2			CPS		CPS	CPS
E1	CPS	DDR5	DDR5	DDR5	DDR5	DDR5
E2				CPS		CPS
F1	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5
F2					CPS	CPS
G1	CPS	DDR5	DDR5	DDR5	DDR5	DDR5
G2				CPS		CPS
H1	DDR5		DDR5	DDR5	DDR5	DDR5
H2					CPS	CPS

2 CPU Configuration (DDR5+CPS)

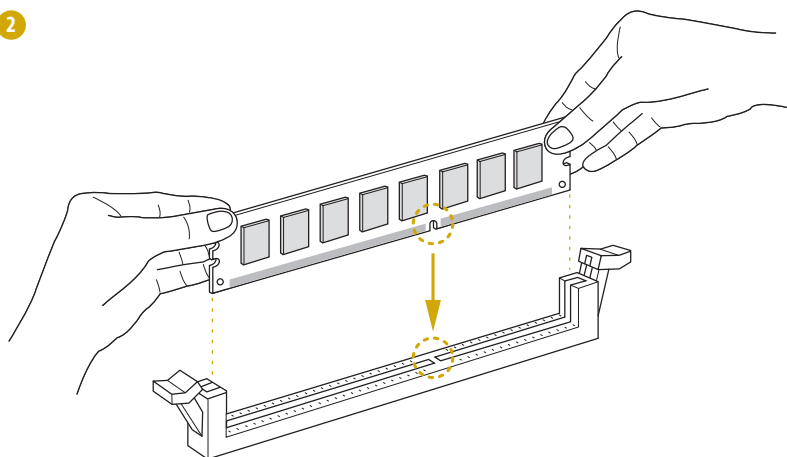
CPU0						
DDR5 + CPS	8 DDR5 + 8 CPS	12 DDR5 + 2 CPS	16 DDR5 + 2 CPS	16 DDR5 + 8 CPS	16 DDR5 + 8 CPS	16 DDR5 + 16 CPS
A1	CPS	DDR5	DDR5	DDR5	DDR5	DDR5
A2				CPS		CPS
B1	DDR5	CPS	DDR5	DDR5	DDR5	DDR5
B2					CPS	CPS
C1	CPS	DDR5	DDR5	DDR5	DDR5	DDR5
C2				CPS		CPS
D1	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5
D2			CPS		CPS	CPS
E1	CPS	DDR5	DDR5	DDR5	DDR5	DDR5
E2				CPS		CPS
F1	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5
F2					CPS	CPS
G1	CPS	DDR5	DDR5	DDR5	DDR5	DDR5
G2				CPS		CPS
H1	DDR5		DDR5	DDR5	DDR5	DDR5
H2					CPS	CPS

CPU1							
		DDR5 + CPS	8 DDR5 + 8 CPS	12 DDR5 + 2 CPS	16 DDR5 + 2 CPS	16 DDR5 + 8 CPS	16 DDR5 + 16 CPS
R1.02	R1.03						
I1	A1	CPS	DDR5	DDR5	DDR5	DDR5	DDR5
I2	A2				CPS		CPS
J1	B1	DDR5	CPS	DDR5	DDR5	DDR5	DDR5
J2	B2					CPS	CPS
K1	C1	CPS	DDR5	DDR5	DDR5	DDR5	DDR5
K2	C2				CPS		CPS
L1	D1	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5
L2	D2			CPS		CPS	CPS
M1	E1	CPS	DDR5	DDR5	DDR5	DDR5	DDR5
M2	E2				CPS		CPS
N1	F1	DDR5	DDR5	DDR5	DDR5	DDR5	DDR5
N2	F2					CPS	CPS
O1	G1	CPS	DDR5	DDR5	DDR5	DDR5	DDR5
O2	G2				CPS		CPS
P1	H1	DDR5		DDR5	DDR5	DDR5	DDR5
P2	H1					CPS	CPS

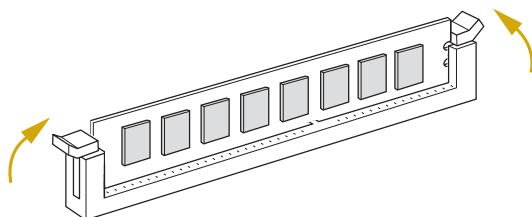
1



2

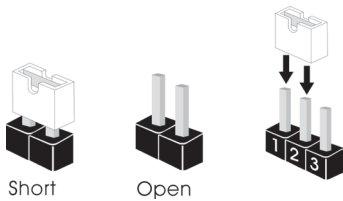


3



2.5 Jumper Setup

The illustration shows how jumpers are setup. When the jumper cap is placed on the pins, the jumper is “Short”. If no jumper cap is placed on the pins, the jumper is “Open”. The illustration shows a 3-pin jumper whose pin1 and pin2 are “Short” when a jumper cap is placed on these 2 pins.



M.2 Signal Source
Selection Jumper
(3-pin M2_NV_SEL1)
(see p.6, No. 57)



RDS (x2) + M.2_1 (x2)



M.2_1 (x4) (Default)

NCSI Mode Jumper
(3-pin NCSI_SEL1)
(see p.6, No. 62)



NCSI to I350 (Default)



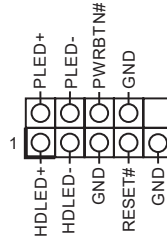
Share to NCSI Header

2.6 Onboard Headers and Connectors



Onboard headers and connectors are NOT jumpers. Do NOT place jumper caps over these headers and connectors. Placing jumper caps over the headers and connectors will cause permanent damage to the motherboard.

System Panel Header
(9-pin PANEL1)
(see p.6, No.45)



Connect the power switch, reset switch and system status indicator on the chassis to this header according to the pin assignments. Particularly note the positive and negative pins before connecting the cables.



PWRBTN (Power Switch):
Connect to the power switch on the chassis front panel and configure the way to turn off the system using the power switch.

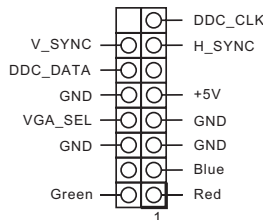
RESET (Reset Switch):
Connect to the reset switch on the chassis front panel. Press the reset switch to restart the computer if the computer freezes and fails to perform a normal restart.

PLED (System Power LED):
Connect to the power status indicator on the chassis front panel. The LED is on when the system is operating. The LED is off when the system is in S4 sleep state or powered off (S5).

HDLED (Hard Drive Activity LED):
Connect to the hard drive activity LED on the chassis front panel. The LED is on when the hard drive is reading or writing data.

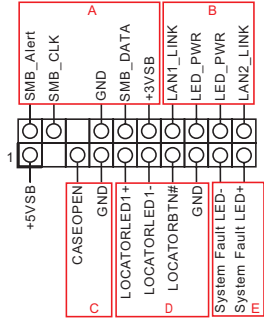
The front panel design may differ by chassis. A front panel module mainly consists of power switch, reset switch, power LED, hard drive activity LED, speaker and etc. When connecting the chassis front panel module to this header, make sure the wire assignments and the pin assignments are matched correctly.

Front VGA Header
(15-pin FRNT_VGA1)
(see p.6, No. 66)



Please connect either end of VGA cable to VGA header.

Auxiliary Panel Header
(18-pin AUX PANEL1)
(see p.6, No.47)



This header supports multiple functions on the front panel, including the front panel SMB, internet status indicator and chassis intrusion pin.



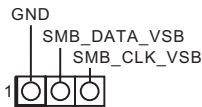
- A. Front panel SMBus connecting pin (6-1 pin FPSMB):**
This header allows user to connect SMBus (System Management Bus) equipment. It can be used for communication between peripheral equipment in the system, which has slower transmission rates, and power management equipment.
- B. Internet status indicator (4-pin LAN, LED):**
This header allows user to use the Gigabit internet indicator cable to connect to the LAN status indicator. When this indicator flickers, it means that the internet is properly connected.
- C. Chassis intrusion pin (2-pin CHASSIS):**
This header is provided for host computer chassis with chassis intrusion detection designs. In addition, it must also work with external detection equipment, such as a chassis intrusion detection sensor or a microswitch. When this function is activated, if any chassis component movement occurs, the sensor will immediately detect it and send a signal to this header, and the system will then record this chassis intrusion event. The default setting is set to the CASEOPEN and GND pin; this function is off.
- D. Locator LED (4-pin LOCATOR):**
This header is for the locator switch and LED on the front panel.
- E. System Fault LED (2-pin SYSTEM STATUS):**
This header is for the Fault LED on the system.

Non Maskable Interrupt
Button Header
(NMI_BTN1)
(see p.6, No.46)



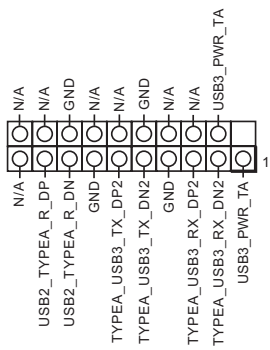
Please connect a NMI device to this header.

PWM Configuration
Header
(3-pin PWM_CFG1)
(see p.6, No.53)



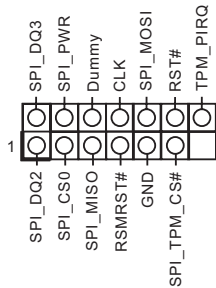
This header is used for PWM configurations.

USB 3.2 Gen1 Header
(19-pin USB3_1_2)
(see p.6, No.48)



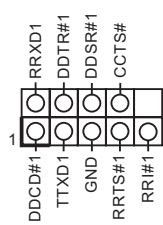
Besides two default USB 3.2 Gen1 ports on the I/O panel, there is one USB 3.2 Gen1 header on this motherboard. This USB 3.2 Gen1 header can support two USB 3.2 Gen1 ports.

SPI TPM Header
(13-pin TPM1)
(see p.6, No.59)



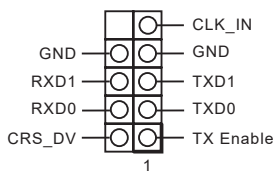
This connector supports SPI Trusted Platform Module (TPM) system, which can securely store keys, digital certificates, passwords, and data. A TPM system also helps enhance network security, protects digital identities, and ensures platform integrity.

COM Port Header
(9-pin COM1)
(see p.6, No.9)



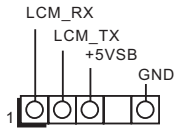
This COM1 header supports a serial port module.

Network Controller Side-band Interface Header
(9-pin NCSI1)
(see p.6, No.65)



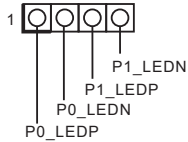
The onboard NCSI header is used for external connections..

Liquid Crystal Module
Header
(4-pin LCM1)
(see p.6, No. 55)



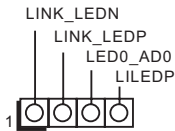
This header is used for extended Liquid Crystal Module(LCM) on the front panel of a server system.

Rear Panel LAN LED
(2-pin RL_LED1)
(see p.6, No. 56)



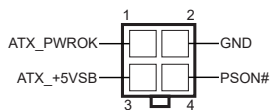
This header is used for extended LAN LED on the rear panel of a server system.

IPMI LAN LED Header
(4-pin IPMI_LED1)
(see p.6, No. 54)



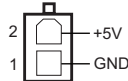
This header is used to connect to the LED indicators on the chassis.

Micro-Fit Power
Connector
(4-pin ATX4PIN1)
(see p.6, No. 4)



The motherboard provides one 4-pin power/signal connector which is a required input for ATX power source. When using ATX power, it is necessary to use a 24pin to 4pin power cable to connect between the 24pin power connector of PSU and the ATX4PIN1 connector on the motherboard for power supply and signal communication.

HDD Backplane Power
Connector
(2-pin BP_PWR1)
(see p.6, No. 44)



Please connect a 2-pin power cable to this connector to connect a HDD.

ATX 12V Power

Connectors

(8-pin ATX12V1)

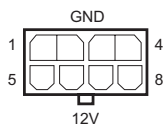
(see p.6, No.3)

(8-pin ATX12V2)

(see p.6, No.5)

(8-pin ATX12V3)

(see p.6, No.7)



This motherboard provides six 8-pin ATX 12V power connectors.

(8-pin ATX12V4

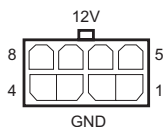
(see p.6, No.40)

(8-pin ATX12V5

(see p.6, No.43)

(8-pin ATX12V6

(see p.6, No.42)



System Fan Headers

(6-pin FAN1)

(see p.6, No.2)

(6-pin FAN2)

(see p.6, No.6)

(6-pin FAN3)

(see p.6, No.8)

(6-pin FAN4)

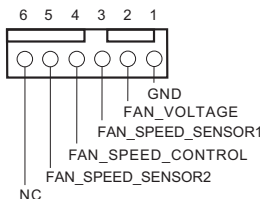
(see p.6, No.41)

(6-pin FAN5)

(see p.6, No.51)

(6-pin FAN6)

(see p.6, No.49)

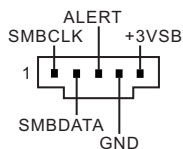


Please connect fan cables to the fan connectors and match the black wire to the ground pin. All fans support Fan Control. The fan max. current is 5A and the max. power is 60Watts.

PSU SMBus

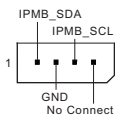
(PSU_SMB1)

(see p.6, No.1)



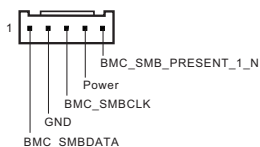
PSU SMBus monitors the status of the power supply, fan and system temperature.

Intelligent Platform
Management Bus header
(4-pin IPMB_1)
(see p.6, No.52)



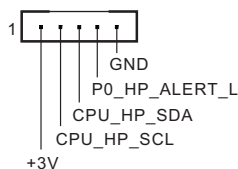
This 4-pin connector is used to provide a cabled base-board or front panel connection for value added features and 3rd-party add-in cards, such as Emergency Management cards, that provide management features using the IPMB.

BMC SMBus Headers
(5-pin BMC_SMB1)
(see p.6, No.70)
(5-pin BMC_SMB2)
(see p.6, No.69)
(5-pin BMC_SMB3)
(see p.6, No.68)



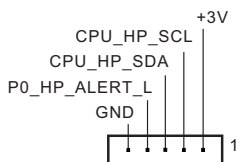
These headers are used for the SM BUS devices.

Backplane PCI Express
Hot-Plug Connectors
(5-pin CPU0_HSBP1)
(see p.6, No.39)



This header is used for the hot plug feature of HDDs on the backplane.

(5-pin CPU1_HSBP1)
(see p.6, No.10)

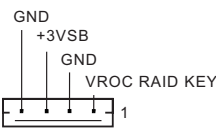


Clear CMOS Pad
(CLRMOS1)
(see p.6, No.67)



CLRMOS1 allows user to clear the data in CMOS. To clear CMOS, take out the CMOS battery and short the Clear CMOS Pad.

Virtual RAID On CPU
Header
(4-pin RAID_1)
(see p.6, No.50)



This connector supports Intel®
Virtual RAID on CPU and
NVME/AHCI RAID on CPU
PCIE.

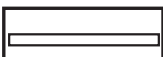
With the introduction of the Intel VROC product, there are three modes of operation:

SKU	HW key required	Key features
Pass-thru	Not needed	• Pass-thru only (no RAID) • LED Management • Hot Plug Support • RAID 0 support for Intel Fultondale NVMe SSDs
Standard	VROCSTANMOD	• Pass-thru SKU features • RAID 0, 1, 10
Premium	VROCPREMMOD	• Standard SKU features • RAID 5
ISS	VROCISSDMOD	• RAID 5 Write Hole Closure

*Only Intel SSDs are supported.
*For further details on VROC, please refer to the official information released by Intel.

MCIO Connectors

Right-Angle:



These connectors are used for the PCIE devices.

(MCIO1)

(see p.6, No.35)

(MCIO2)

(see p.6, No.33)

(MCIO3)

(see p.6, No.31)

(MCIO4)

(see p.6, No.30)

(MCIO5)

(see p.6, No.28)

(MCIO6)

(see p.6, No.26)

(MCIO11)

(see p.6, No.24)

(MCIO12)

(see p.6, No.23)

(MCIO13)

(see p.6, No.21)

(MCIO14)

(see p.6, No.19)

(MCIO15)

(see p.6, No.17)

(MCIO16)

(see p.6, No.16)

Vertical:

(MCIO7)

(see p.6, No.60)

(MCIO8)

(see p.6, No.61)

(MCIO9)

(see p.6, No.38)

(MCIO10)

(see p.6, No.37)

(MCIO17)

(see p.6, No.11)

(MCIO18)

(see p.6, No.12)

(MCIO19)

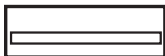
(see p.6, No.63)

(MCIO20)

(see p.6, No.64)

(MCIO21)

(see p.6, No.15)



These connectors are used for the PCIe devices.

MCIO1 Pin Definition [CPU0]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE0_RX_DP0	B2	PE0_TX_DP0
A3	PE0_RX_DN0	B3	PE0_TX_DN0
A4	GND	B4	GND
A5	PE0_RX_DP1	B5	PE0_TX_DP1
A6	PE0_RX_DN1	B6	PE0_TX_DN1
A7	GND	B7	GND
A8	B12_IFDET1_MCIO1	B8	SMB_MCIO1_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO1_SDA1
A10	GND	B10	GND
A11	CLK_MCIO1_DP1	B11	MCIO_1_PERST0_N
A12	CLK_MCIO1_DN1	B12	MCIO_1_PRSENT0_N
A13	GND	B13	GND
A14	PE0_RX_DP2	B14	PE0_TX_DP2
A15	PE0_RX_DN2	B15	PE0_TX_DN2
A16	GND	B16	GND
A17	PE0_RX_DP3	B17	PE0_TX_DP3
A18	PE0_RX_DN3	B18	PE0_TX_DN3
A19	GND	B19	GND
A20	PE0_RX_DP4	B20	PE0_TX_DP4
A21	PE0_RX_DN4	B21	PE0_TX_DN4
A22	GND	B22	GND
A23	PE0_RX_DP5	B23	PE0_TX_DP5
A24	PE0_RX_DN5	B24	PE0_TX_DN5
A25	GND	B25	GND
A26	B30_IFDET2_MCIO1	B26	SMB_MCIO1_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO1_SDA2
A28	GND	B28	GND
A29	CLK_MCIO1_DP2	B29	MCIO_1_PERST1_N
A30	CLK_MCIO1_DN2	B30	MCIO_1_PRSENT1_N
A31	GND	B31	GND
A32	PE0_RX_DP6	B32	PE0_TX_DP6
A33	PE0_RX_DN6	B33	PE0_TX_DN6
A34	GND	B34	GND
A35	PE0_RX_DP7	B35	PE0_TX_DP7
A36	PE0_RX_DN7	B36	PE0_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO2 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE0_RX_DP8	B2	PE0_TX_DP8
A3	PE0_RX_DN8	B3	PE0_TX_DN8
A4	GND	B4	GND
A5	PE0_RX_DP9	B5	PE0_TX_DP9
A6	PE0_RX_DN9	B6	PE0_TX_DN9
A7	GND	B7	GND
A8	B12_IFDET1_MCIO2	B8	SMB_MCIO2_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO2_SDA1
A10	GND	B10	GND
A11	CLK_MCIO2_DP1	B11	MCIO_2_PERST0_N
A12	CLK_MCIO2_DN1	B12	MCIO_2_PRSENT0_N
A13	GND	B13	GND
A14	PE0_RX_DP10	B14	PE0_TX_DP10
A15	PE0_RX_DN10	B15	PE0_TX_DN10
A16	GND	B16	GND
A17	PE0_RX_DP11	B17	PE0_TX_DP11
A18	PE0_RX_DN11	B18	PE0_TX_DN11
A19	GND	B19	GND
A20	PE0_RX_DP12	B20	PE0_TX_DP12
A21	PE0_RX_DN12	B21	PE0_TX_DN12
A22	GND	B22	GND
A23	PE0_RX_DP13	B23	PE0_TX_DP13
A24	PE0_RX_DN13	B24	PE0_TX_DN13
A25	GND	B25	GND
A26	B30_IFDET2_MCIO2	B26	SMB_MCIO2_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO2_SDA2
A28	GND	B28	GND
A29	CLK_MCIO2_DP2	B29	MCIO_2_PERST1_N
A30	CLK_MCIO2_DN2	B30	MCIO_2_PRSENT1_N
A31	GND	B31	GND
A32	PE0_RX_DP14	B32	PE0_TX_DP14
A33	PE0_RX_DN14	B33	PE0_TX_DN14
A34	GND	B34	GND
A35	PE0_RX_DP15	B35	PE0_TX_DP15
A36	PE0_RX_DN15	B36	PE0_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO3 Pin Definition [CPU0]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE1_RX_DP0	B2	PE1_TX_DP0
A3	PE1_RX_DN0	B3	PE1_TX_DN0
A4	GND	B4	GND
A5	PE1_RX_DP1	B5	PE1_TX_DP1
A6	PE1_RX_DN1	B6	PE1_TX_DN1
A7	GND	B7	GND
A8	B12_IFDET1_MCIO3	B8	SMB_MCIO3_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO3_SDA1
A10	GND	B10	GND
A11	CLK_MCIO3_DP1	B11	MCIO_3_PERST0_N
A12	CLK_MCIO3_DN1	B12	MCIO_3_PRSENT0_N
A13	GND	B13	GND
A14	PE1_RX_DP2	B14	PE1_TX_DP2
A15	PE1_RX_DN2	B15	PE1_TX_DN2
A16	GND	B16	GND
A17	PE1_RX_DP3	B17	PE1_TX_DP3
A18	PE1_RX_DN3	B18	PE1_TX_DN3
A19	GND	B19	GND
A20	PE1_RX_DP4	B20	PE1_TX_DP4
A21	PE1_RX_DN4	B21	PE1_TX_DN4
A22	GND	B22	GND
A23	PE1_RX_DP5	B23	PE1_TX_DP5
A24	PE1_RX_DN5	B24	PE1_TX_DN5
A25	GND	B25	GND
A26	B30_IFDET2_MCIO3	B26	SMB_MCIO3_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO3_SDA2
A28	GND	B28	GND
A29	CLK_MCIO3_DP2	B29	MCIO_3_PERST1_N
A30	CLK_MCIO3_DN2	B30	MCIO_3_PRSENT1_N
A31	GND	B31	GND
A32	PE1_RX_DP6	B32	PE1_TX_DP6
A33	PE1_RX_DN6	B33	PE1_TX_DN6
A34	GND	B34	GND
A35	PE1_RX_DP7	B35	PE1_TX_DP7
A36	PE1_RX_DN7	B36	PE1_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO4 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE1_RX_DP8	B2	PE1_TX_DP8
A3	PE1_RX_DN8	B3	PE1_TX_DN8
A4	GND	B4	GND
A5	PE1_RX_DP9	B5	PE1_TX_DP9
A6	PE1_RX_DN9	B6	PE1_TX_DN9
A7	GND	B7	GND
A8	B12_IFDET1_MCIO4	B8	SMB_MCIO4_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO4_SDA1
A10	GND	B10	GND
A11	CLK_MCIO4_DP1	B11	MCIO_4_PERST0_N
A12	CLK_MCIO4_DN1	B12	MCIO_4_PRSENT0_N
A13	GND	B13	GND
A14	PE1_RX_DP10	B14	PE1_TX_DP10
A15	PE1_RX_DN10	B15	PE1_TX_DN10
A16	GND	B16	GND
A17	PE1_RX_DP11	B17	PE1_TX_DP11
A18	PE1_RX_DN11	B18	PE1_TX_DN11
A19	GND	B19	GND
A20	PE1_RX_DP12	B20	PE1_TX_DP12
A21	PE1_RX_DN12	B21	PE1_TX_DN12
A22	GND	B22	GND
A23	PE1_RX_DP13	B23	PE1_TX_DP13
A24	PE1_RX_DN13	B24	PE1_TX_DN13
A25	GND	B25	GND
A26	B30_IFDET2_MCIO4	B26	SMB_MCIO4_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO4_SDA2
A28	GND	B28	GND
A29	CLK_MCIO4_DP2	B29	MCIO_4_PERST1_N
A30	CLK_MCIO4_DN2	B30	MCIO_4_PRSENT1_N
A31	GND	B31	GND
A32	PE1_RX_DP14	B32	PE1_TX_DP14
A33	PE1_RX_DN14	B33	PE1_TX_DN14
A34	GND	B34	GND
A35	PE1_RX_DP15	B35	PE1_TX_DP15
A36	PE1_RX_DN15	B36	PE1_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO5 Pin Definition [CPU0]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE2_RX_DP0	B2	PE2_TX_DP0
A3	PE2_RX_DN0	B3	PE2_TX_DN0
A4	GND	B4	GND
A5	PE2_RX_DP1	B5	PE2_TX_DP1
A6	PE2_RX_DN1	B6	PE2_TX_DN1
A7	GND	B7	GND
A8	B12_IFDET1_MCIO5	B8	SMB_MCIO5_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO5_SDA1
A10	GND	B10	GND
A11	CLK_MCIO5_DP1	B11	MCIO_5_PERST0_N
A12	CLK_MCIO5_DN1	B12	MCIO_5_PRSENT0_N
A13	GND	B13	GND
A14	PE2_RX_DP2	B14	PE2_TX_DP2
A15	PE2_RX_DN2	B15	PE2_TX_DN2
A16	GND	B16	GND
A17	PE2_RX_DP3	B17	PE2_TX_DP3
A18	PE2_RX_DN3	B18	PE2_TX_DN3
A19	GND	B19	GND
A20	PE2_RX_DP4	B20	PE2_TX_DP4
A21	PE2_RX_DN4	B21	PE2_TX_DN4
A22	GND	B22	GND
A23	PE2_RX_DP5	B23	PE2_TX_DP5
A24	PE2_RX_DN5	B24	PE2_TX_DN5
A25	GND	B25	GND
A26	B30_IFDET2_MCIO5	B26	SMB_MCIO5_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO5_SDA2
A28	GND	B28	GND
A29	CLK_MCIO5_DP2	B29	MCIO_5_PERST1_N
A30	CLK_MCIO5_DN2	B30	MCIO_5_PRSENT1_N
A31	GND	B31	GND
A32	PE2_RX_DP6	B32	PE2_TX_DP6
A33	PE2_RX_DN6	B33	PE2_TX_DN6
A34	GND	B34	GND
A35	PE2_RX_DP7	B35	PE2_TX_DP7
A36	PE2_RX_DN7	B36	PE2_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO6 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE2_RX_DP8	B2	PE2_TX_DP8
A3	PE2_RX_DN8	B3	PE2_TX_DN8
A4	GND	B4	GND
A5	PE2_RX_DP9	B5	PE2_TX_DP9
A6	PE2_RX_DN9	B6	PE2_TX_DN9
A7	GND	B7	GND
A8	B12_IFDET1_MCIO6	B8	SMB_MCIO6_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO6_SDA1
A10	GND	B10	GND
A11	CLK_MCIO6_DP1	B11	MCIO_6_PERST0_N
A12	CLK_MCIO6_DN1	B12	MCIO_6_PRSENT0_N
A13	GND	B13	GND
A14	PE2_RX_DP10	B14	PE2_TX_DP10
A15	PE2_RX_DN10	B15	PE2_TX_DN10
A16	GND	B16	GND
A17	PE2_RX_DP11	B17	PE2_TX_DP11
A18	PE2_RX_DN11	B18	PE2_TX_DN11
A19	GND	B19	GND
A20	PE2_RX_DP12	B20	PE2_TX_DP12
A21	PE2_RX_DN12	B21	PE2_TX_DN12
A22	GND	B22	GND
A23	PE2_RX_DP13	B23	PE2_TX_DP13
A24	PE2_RX_DN13	B24	PE2_TX_DN13
A25	GND	B25	GND
A26	B30_IFDET2_MCIO6	B26	SMB_MCIO6_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO6_SDA2
A28	GND	B28	GND
A29	CLK_MCIO6_DP2	B29	MCIO_6_PERST1_N
A30	CLK_MCIO6_DN2	B30	MCIO_6_PRSENT1_N
A31	GND	B31	GND
A32	PE2_RX_DP14	B32	PE2_TX_DP14
A33	PE2_RX_DN14	B33	PE2_TX_DN14
A34	GND	B34	GND
A35	PE2_RX_DP15	B35	PE2_TX_DP15
A36	PE2_RX_DN15	B36	PE2_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO7 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE3_RX_DN15	B2	PE3_TX_DN15
A3	PE3_RX_DP15	B3	PE3_TX_DP15
A4	GND	B4	GND
A5	PE3_RX_DN14	B5	PE3_TX_DN14
A6	PE3_RX_DP14	B6	PE3_TX_DP14
A7	GND	B7	GND
A8	B12_IFDET1_MCIO7	B8	SMB_MCIO7_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO7_SDA1
A10	GND	B10	GND
A11	CLK_MCIO7_DP1	B11	MCIO_7_PERST0_N
A12	CLK_MCIO7_DN1	B12	MCIO_7_PRSENT0_N
A13	GND	B13	GND
A14	PE3_RX_DN13	B14	PE3_TX_DN13
A15	PE3_RX_DP13	B15	PE3_TX_DP13
A16	GND	B16	GND
A17	PE3_RX_DN12	B17	PE3_TX_DN12
A18	PE3_RX_DP12	B18	PE3_TX_DP12
A19	GND	B19	GND
A20	PE3_RX_DN11	B20	PE3_TX_DN11
A21	PE3_RX_DP11	B21	PE3_TX_DP11
A22	GND	B22	GND
A23	PE3_RX_DN10	B23	PE3_TX_DN10
A24	PE3_RX_DP10	B24	PE3_TX_DP10
A25	GND	B25	GND
A26	B30_IFDET2_MCIO7	B26	SMB_MCIO7_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO7_SDA2
A28	GND	B28	GND
A29	CLK_MCIO7_DP2	B29	MCIO_7_PERST1_N
A30	CLK_MCIO7_DN2	B30	MCIO_7_PRSENT1_N
A31	GND	B31	GND
A32	PE3_RX_DN9	B32	PE3_TX_DN9
A33	PE3_RX_DP9	B33	PE3_TX_DP9
A34	GND	B34	GND
A35	PE3_RX_DN8	B35	PE3_TX_DN8
A36	PE3_RX_DP8	B36	PE3_TX_DP8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO8 Pin Definition [CPU0]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE3_RX_DN7	B2	PE3_TX_DN7
A3	PE3_RX_DP7	B3	PE3_TX_DP7
A4	GND	B4	GND
A5	PE3_RX_DN6	B5	PE3_TX_DN6
A6	PE3_RX_DP6	B6	PE3_TX_DP6
A7	GND	B7	GND
A8	B12_IFDET1_MCIO8	B8	SMB_MCIO8_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO8_SDA1
A10	GND	B10	GND
A11	CLK_MCIO8_DP1	B11	MCIO_8_PERST0_N
A12	CLK_MCIO8_DN1	B12	MCIO_8_PRSENT0_N
A13	GND	B13	GND
A14	PE3_RX_DN5	B14	PE3_TX_DN5
A15	PE3_RX_DP5	B15	PE3_TX_DP5
A16	GND	B16	GND
A17	PE3_RX_DN4	B17	PE3_TX_DN4
A18	PE3_RX_DP4	B18	PE3_TX_DP4
A19	GND	B19	GND
A20	PE3_RX_DN3	B20	PE3_TX_DN3
A21	PE3_RX_DP3	B21	PE3_TX_DP3
A22	GND	B22	GND
A23	PE3_RX_DN2	B23	PE3_TX_DN2
A24	PE3_RX_DP2	B24	PE3_TX_DP2
A25	GND	B25	GND
A26	B30_IFDET2_MCIO8	B26	SMB_MCIO8_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO8_SDA2
A28	GND	B28	GND
A29	CLK_MCIO8_DP2	B29	MCIO_8_PERST1_N
A30	CLK_MCIO8_DN2	B30	MCIO_8_PRSENT1_N
A31	GND	B31	GND
A32	PE3_RX_DN1	B32	PE3_TX_DN1
A33	PE3_RX_DP1	B33	PE3_TX_DP1
A34	GND	B34	GND
A35	PE3_RX_DN0	B35	PE3_TX_DN0
A36	PE3_RX_DP0	B36	PE3_TX_DP0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO9 Pin Definition [CPU0]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE4_RX_DP0	B2	PE4_TX_DP0
A3	PE4_RX_DN0	B3	PE4_TX_DN0
A4	GND	B4	GND
A5	PE4_RX_DP1	B5	PE4_TX_DP1
A6	PE4_RX_DN1	B6	PE4_TX_DN1
A7	GND	B7	GND
A8	B12_IFDET1_MCIO9	B8	SMB_MCIO9_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO9_SDA1
A10	GND	B10	GND
A11	CLK_MCIO9_DP1	B11	MCIO_9_PERST#1
A12	CLK_MCIO9_DN1	B12	MCIO_9_PRST#1
A13	GND	B13	GND
A14	PE4_RX_DP2	B14	PE4_TX_DP2
A15	PE4_RX_DN2	B15	PE4_TX_DN2
A16	GND	B16	GND
A17	PE4_RX_DP3	B17	PE4_TX_DP3
A18	PE4_RX_DN3	B18	PE4_TX_DN3
A19	GND	B19	GND
A20	PE4_RX_DP4	B20	PE4_TX_DP4
A21	PE4_RX_DN4	B21	PE4_TX_DN4
A22	GND	B22	GND
A23	PE4_RX_DP5	B23	PE4_TX_DP5
A24	PE4_RX_DN5	B24	PE4_TX_DN5
A25	GND	B25	GND
A26	B30_IFDET2_MCIO9	B26	SMB_MCIO9_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO9_SDA2
A28	GND	B28	GND
A29	CLK_MCIO9_DP2	B29	MCIO_9_PERST#2
A30	CLK_MCIO9_DN2	B30	MCIO_9_PRST#2
A31	GND	B31	GND
A32	PE4_RX_DP6	B32	PE4_TX_DP6
A33	PE4_RX_DN6	B33	PE4_TX_DN6
A34	GND	B34	GND
A35	PE4_RX_DP7	B35	PE4_TX_DP7
A36	PE4_RX_DN7	B36	PE4_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO10 Pin Definition [CPU0]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE4_RX_DP8	B2	PE4_TX_DP8
A3	PE4_RX_DN8	B3	PE4_TX_DN8
A4	GND	B4	GND
A5	PE4_RX_DP9	B5	PE4_TX_DP9
A6	PE4_RX_DN9	B6	PE4_TX_DN9
A7	GND	B7	GND
A8	B12_IFDET1_MCIO10	B8	SMB_MCIO10_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO10_SDA1
A10	GND	B10	GND
A11	CLK_MCIO10_DP1	B11	MCIO_10_PERST0_N
A12	CLK_MCIO10_DN1	B12	MCIO_10_PRSTNT0_N
A13	GND	B13	GND
A14	PE4_RX_DP10	B14	PE4_TX_DP10
A15	PE4_RX_DN10	B15	PE4_TX_DN10
A16	GND	B16	GND
A17	PE4_RX_DP11	B17	PE4_TX_DP11
A18	PE4_RX_DN11	B18	PE4_TX_DN11
A19	GND	B19	GND
A20	PE2_RX_DP12	B20	PE4_TX_DP12
A21	PE2_RX_DN12	B21	PE4_TX_DN12
A22	GND	B22	GND
A23	PE4_RX_DP13	B23	PE4_TX_DP13
A24	PE4_RX_DN13	B24	PE4_TX_DN13
A25	GND	B25	GND
A26	B30_IFDET2_MCIO10	B26	SMB_MCIO10_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO10_SDA2
A28	GND	B28	GND
A29	CLK_MCIO10_DP2	B29	MCIO_10_PERST1_N
A30	CLK_MCIO10_DN2	B30	MCIO_10_PRSTNT1_N
A31	GND	B31	GND
A32	PE4_RX_DP14	B32	PE4_TX_DP14
A33	PE4_RX_DN14	B33	PE4_TX_DN14
A34	GND	B34	GND
A35	PE4_RX_DP15	B35	PE4_TX_DP15
A36	PE4_RX_DN15	B36	PE4_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO11 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE0_RX_DP0	B2	PE0_TX_DP0
A3	PE0_RX_DN0	B3	PE0_TX_DN0
A4	GND	B4	GND
A5	PE0_RX_DP1	B5	PE0_TX_DP1
A6	PE0_RX_DN1	B6	PE0_TX_DN1
A7	GND	B7	GND
A8	B12_IFDET1_MCIO11	B8	SMB_MCIO11_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO11_SDA1
A10	GND	B10	GND
A11	CLK_MCIO11_DP1	B11	MCIO_11_PERST0_N
A12	CLK_MCIO11_DN1	B12	MCIO_11_PRSTNT0_N
A13	GND	B13	GND
A14	PE0_RX_DP2	B14	PE0_TX_DP2
A15	PE0_RX_DN2	B15	PE0_TX_DN2
A16	GND	B16	GND
A17	PE0_RX_DP3	B17	PE0_TX_DP3
A18	PE0_RX_DN3	B18	PE0_TX_DN3
A19	GND	B19	GND
A20	PE0_RX_DP4	B20	PE0_TX_DP4
A21	PE0_RX_DN4	B21	PE0_TX_DN4
A22	GND	B22	GND
A23	PE0_RX_DP5	B23	PE0_TX_DP5
A24	PE0_RX_DN5	B24	PE0_TX_DN5
A25	GND	B25	GND
A26	B30_IFDET2_MCIO11	B26	SMB_MCIO11_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO11_SDA2
A28	GND	B28	GND
A29	CLK_MCIO11_DP2	B29	MCIO_11_PERST1_N
A30	CLK_MCIO11_DN2	B30	MCIO_11_PRSTNT1_N
A31	GND	B31	GND
A32	PE0_RX_DP6	B32	PE0_TX_DP6
A33	PE0_RX_DN6	B33	PE0_TX_DN6
A34	GND	B34	GND
A35	PE0_RX_DP7	B35	PE0_TX_DP7
A36	PE0_RX_DN7	B36	PE0_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO12 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE0_RX_DP8	B2	PE0_TX_DP8
A3	PE0_RX_DN8	B3	PE0_TX_DN8
A4	GND	B4	GND
A5	PE0_RX_DP9	B5	PE0_TX_DP9
A6	PE0_RX_DN9	B6	PE0_TX_DN9
A7	GND	B7	GND
A8	B12_IFDET1_MCIO12	B8	SMB_MCIO12_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO12_SDA1
A10	GND	B10	GND
A11	CLK_MCIO12_DP1	B11	MCIO_12_PERST0_N
A12	CLK_MCIO12_DN1	B12	MCIO_12_PRSENT0_N
A13	GND	B13	GND
A14	PE0_RX_DP10	B14	PE0_TX_DP10
A15	PE0_RX_DN10	B15	PE0_TX_DN10
A16	GND	B16	GND
A17	PE0_RX_DP11	B17	PE0_TX_DP11
A18	PE0_RX_DN11	B18	PE0_TX_DN11
A19	GND	B19	GND
A20	PE0_RX_DP12	B20	PE0_TX_DP12
A21	PE0_RX_DN12	B21	PE0_TX_DN12
A22	GND	B22	GND
A23	PE0_RX_DP13	B23	PE0_TX_DP13
A24	PE0_RX_DN13	B24	PE0_TX_DN13
A25	GND	B25	GND
A26	B30_IFDET2_MCIO12	B26	SMB_MCIO12_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO12_SDA2
A28	GND	B28	GND
A29	CLK_MCIO12_DP2	B29	MCIO_12_PERST1_N
A30	CLK_MCIO12_DN2	B30	MCIO_12_PRSENT1_N
A31	GND	B31	GND
A32	PE0_RX_DP14	B32	PE0_TX_DP14
A33	PE0_RX_DN14	B33	PE0_TX_DN14
A34	GND	B34	GND
A35	PE0_RX_DP15	B35	PE0_TX_DP15
A36	PE0_RX_DN15	B36	PE0_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO13 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE1_RX_DP0	B2	PE1_TX_DP0
A3	PE1_RX_DN0	B3	PE1_TX_DN0
A4	GND	B4	GND
A5	PE1_RX_DP1	B5	PE1_TX_DP1
A6	PE1_RX_DN1	B6	PE1_TX_DN1
A7	GND	B7	GND
A8	B12_IFDET1_MCIO13	B8	SMB_MCIO13_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO13_SDA1
A10	GND	B10	GND
A11	CLK_MCIO13_DP1	B11	MCIO_13_PERST0_N
A12	CLK_MCIO13_DN1	B12	MCIO_13_PRSENT0_N
A13	GND	B13	GND
A14	PE1_RX_DP2	B14	PE1_TX_DP2
A15	PE1_RX_DN2	B15	PE1_TX_DN2
A16	GND	B16	GND
A17	PE1_RX_DP3	B17	PE1_TX_DP3
A18	PE1_RX_DN3	B18	PE1_TX_DN3
A19	GND	B19	GND
A20	PE1_RX_DP4	B20	PE1_TX_DP4
A21	PE1_RX_DN4	B21	PE1_TX_DN4
A22	GND	B22	GND
A23	PE1_RX_DP5	B23	PE1_TX_DP5
A24	PE1_RX_DN5	B24	PE1_TX_DN5
A25	GND	B25	GND
A26	B30_IFDET2_MCIO13	B26	SMB_MCIO13_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO13_SDA2
A28	GND	B28	GND
A29	CLK_MCIO13_DP2	B29	MCIO_13_PERST1_N
A30	CLK_MCIO13_DN2	B30	MCIO_13_PRSENT1_N
A31	GND	B31	GND
A32	PE1_RX_DP6	B32	PE1_TX_DP6
A33	PE1_RX_DN6	B33	PE1_TX_DN6
A34	GND	B34	GND
A35	PE1_RX_DP7	B35	PE1_TX_DP7
A36	PE1_RX_DN7	B36	PE1_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO14 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE1_RX_DP8	B2	PE1_TX_DP8
A3	PE1_RX_DN8	B3	PE1_TX_DN8
A4	GND	B4	GND
A5	PE1_RX_DP9	B5	PE1_TX_DP9
A6	PE1_RX_DN9	B6	PE1_TX_DN9
A7	GND	B7	GND
A8	B12_IFDET1_MCIO14	B8	SMB_MCIO14_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO14_SDA1
A10	GND	B10	GND
A11	CLK_MCIO14_DP1	B11	MCIO_14_PERST0_N
A12	CLK_MCIO14_DN1	B12	MCIO_14_PRSENT0_N
A13	GND	B13	GND
A14	PE1_RX_DP10	B14	PE1_TX_DP10
A15	PE1_RX_DN10	B15	PE1_TX_DN10
A16	GND	B16	GND
A17	PE1_RX_DP11	B17	PE1_TX_DP11
A18	PE1_RX_DN11	B18	PE1_TX_DN11
A19	GND	B19	GND
A20	PE1_RX_DP12	B20	PE1_TX_DP12
A21	PE1_RX_DN12	B21	PE1_TX_DN12
A22	GND	B22	GND
A23	PE1_RX_DP13	B23	PE1_TX_DP13
A24	PE1_RX_DN13	B24	PE1_TX_DN13
A25	GND	B25	GND
A26	B30_IFDET2_MCIO14	B26	SMB_MCIO14_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO14_SDA2
A28	GND	B28	GND
A29	CLK_MCIO14_DP2	B29	MCIO_14_PERST1_N
A30	CLK_MCIO14_DN2	B30	MCIO_14_PRSENT1_N
A31	GND	B31	GND
A32	PE1_RX_DP14	B32	PE1_TX_DP14
A33	PE1_RX_DN14	B33	PE1_TX_DN14
A34	GND	B34	GND
A35	PE1_RX_DP15	B35	PE1_TX_DP15
A36	PE1_RX_DN15	B36	PE1_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO15 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE2_RX_DP0	B2	PE2_TX_DP0
A3	PE2_RX_DN0	B3	PE2_TX_DN0
A4	GND	B4	GND
A5	PE2_RX_DP1	B5	PE2_TX_DP1
A6	PE2_RX_DN1	B6	PE2_TX_DN1
A7	GND	B7	GND
A8	B12_IFDET1_MCIO15	B8	SMB_MCIO15_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO15_SDA1
A10	GND	B10	GND
A11	CLK_MCIO15_DP1	B11	MCIO_15_PERST0_N
A12	CLK_MCIO15_DN1	B12	MCIO_15_PRST0_N
A13	GND	B13	GND
A14	PE2_RX_DP2	B14	PE2_TX_DP2
A15	PE2_RX_DN2	B15	PE2_TX_DN2
A16	GND	B16	GND
A17	PE2_RX_DP3	B17	PE2_TX_DP3
A18	PE2_RX_DN3	B18	PE2_TX_DN3
A19	GND	B19	GND
A20	PE2_RX_DP4	B20	PE2_TX_DP4
A21	PE2_RX_DN4	B21	PE2_TX_DN4
A22	GND	B22	GND
A23	PE2_RX_DP5	B23	PE2_TX_DP5
A24	PE2_RX_DN5	B24	PE2_TX_DN5
A25	GND	B25	GND
A26	B30_IFDET2_MCIO15	B26	SMB_MCIO15_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO15_SDA2
A28	GND	B28	GND
A29	CLK_MCIO15_DP2	B29	MCIO_15_PERST1_N
A30	CLK_MCIO15_DN2	B30	MCIO_15_PRST1_N
A31	GND	B31	GND
A32	PE2_RX_DP6	B32	PE2_TX_DP6
A33	PE2_RX_DN6	B33	PE2_TX_DN6
A34	GND	B34	GND
A35	PE2_RX_DP7	B35	PE2_TX_DP7
A36	PE2_RX_DN7	B36	PE2_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO16 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE2_RX_DP8	B2	PE2_TX_DP8
A3	PE2_RX_DN8	B3	PE2_TX_DN8
A4	GND	B4	GND
A5	PE2_RX_DP9	B5	PE2_TX_DP9
A6	PE2_RX_DN9	B6	PE2_TX_DN9
A7	GND	B7	GND
A8	B12_IFDET1_MCIO16	B8	SMB_MCIO16_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO16_SDA1
A10	GND	B10	GND
A11	CLK_MCIO16_DP1	B11	MCIO_16_PERST0_N
A12	CLK_MCIO16_DN1	B12	MCIO_16_PRSTNT0_N
A13	GND	B13	GND
A14	PE2_RX_DP10	B14	PE2_TX_DP10
A15	PE2_RX_DN10	B15	PE2_TX_DN10
A16	GND	B16	GND
A17	PE2_RX_DP11	B17	PE2_TX_DP11
A18	PE2_RX_DN11	B18	PE2_TX_DN11
A19	GND	B19	GND
A20	PE2_RX_DP12	B20	PE2_TX_DP12
A21	PE2_RX_DN12	B21	PE2_TX_DN12
A22	GND	B22	GND
A23	PE2_RX_DP13	B23	PE2_TX_DP13
A24	PE2_RX_DN13	B24	PE2_TX_DN13
A25	GND	B25	GND
A26	B30_IFDET2_MCIO16	B26	SMB_MCIO16_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO16_SDA2
A28	GND	B28	GND
A29	CLK_MCIO16_DP2	B29	MCIO_16_PERST1_N
A30	CLK_MCIO16_DN2	B30	MCIO_16_PRSTNT1_N
A31	GND	B31	GND
A32	PE2_RX_DP14	B32	PE2_TX_DP14
A33	PE2_RX_DN14	B33	PE2_TX_DN14
A34	GND	B34	GND
A35	PE2_RX_DP15	B35	PE2_TX_DP15
A36	PE2_RX_DN15	B36	PE2_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO17 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE3_RX_DP0	B2	PE3_TX_DP0
A3	PE3_RX_DN0	B3	PE3_TX_DN0
A4	GND	B4	GND
A5	PE3_RX_DP1	B5	PE3_TX_DP1
A6	PE3_RX_DN1	B6	PE3_TX_DN1
A7	GND	B7	GND
A8	B12_IFDET1_MCIO17	B8	SMB_MCIO17_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO17_SDA1
A10	GND	B10	GND
A11	CLK_MCIO17_DP1	B11	MCIO_17_PERST0_N
A12	CLK_MCIO17_DN1	B12	MCIO_17_PRSTNT0_N
A13	GND	B13	GND
A14	PE3_RX_DP2	B14	PE3_TX_DP2
A15	PE3_RX_DN2	B15	PE3_TX_DN2
A16	GND	B16	GND
A17	PE3_RX_DP3	B17	PE3_TX_DP3
A18	PE3_RX_DN3	B18	PE3_TX_DN3
A19	GND	B19	GND
A20	PE3_RX_DP4	B20	PE3_TX_DP4
A21	PE3_RX_DN4	B21	PE3_TX_DN4
A22	GND	B22	GND
A23	PE3_RX_DP5	B23	PE3_TX_DP5
A24	PE3_RX_DN5	B24	PE3_TX_DN5
A25	GND	B25	GND
A26	B30_IFDET2_MCIO17	B26	SMB_MCIO17_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO17_SDA2
A28	GND	B28	GND
A29	CLK_MCIO17_DP2	B29	MCIO_17_PERST1_N
A30	CLK_MCIO17_DN2	B30	MCIO_17_PRSTNT1_N
A31	GND	B31	GND
A32	PE3_RX_DP6	B32	PE3_TX_DP6
A33	PE3_RX_DN6	B33	PE3_TX_DN6
A34	GND	B34	GND
A35	PE3_RX_DP7	B35	PE3_TX_DP7
A36	PE3_RX_DN7	B36	PE3_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO18 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE3_RX_DP8	B2	PE3_TX_DP8
A3	PE3_RX_DN8	B3	PE3_TX_DN8
A4	GND	B4	GND
A5	PE3_RX_DP9	B5	PE3_TX_DP9
A6	PE3_RX_DN9	B6	PE3_TX_DN9
A7	GND	B7	GND
A8	B12_IFDET1_MCIO18	B8	SMB_MCIO18_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO18_SDA1
A10	GND	B10	GND
A11	CLK_MCIO18_DP1	B11	MCIO_18_PERST0_N
A12	CLK_MCIO18_DN1	B12	MCIO_18_PRSENT0_N
A13	GND	B13	GND
A14	PE3_RX_DP10	B14	PE3_TX_DP10
A15	PE3_RX_DN10	B15	PE3_TX_DN10
A16	GND	B16	GND
A17	PE3_RX_DP11	B17	PE3_TX_DP11
A18	PE3_RX_DN11	B18	PE3_TX_DN11
A19	GND	B19	GND
A20	PE3_RX_DP12	B20	PE3_TX_DP12
A21	PE3_RX_DN12	B21	PE3_TX_DN12
A22	GND	B22	GND
A23	PE3_RX_DP13	B23	PE3_TX_DP13
A24	PE3_RX_DN13	B24	PE3_TX_DN13
A25	GND	B25	GND
A26	B30_IFDET2_MCIO18	B26	SMB_MCIO18_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO18_SDA2
A28	GND	B28	GND
A29	CLK_MCIO18_DP2	B29	MCIO_18_PERST1_N
A30	CLK_MCIO18_DN2	B30	MCIO_18_PRSENT1_N
A31	GND	B31	GND
A32	PE3_RX_DP14	B32	PE3_TX_DP14
A33	PE3_RX_DN14	B33	PE3_TX_DN14
A34	GND	B34	GND
A35	PE3_RX_DP15	B35	PE3_TX_DP15
A36	PE3_RX_DN15	B36	PE3_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO19 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	PE4_RX_DP0	B2	PE4_TX_DP0
A3	PE4_RX_DN0	B3	PE4_TX_DN0
A4	GND	B4	GND
A5	PE4_RX_DP1	B5	PE4_TX_DP1
A6	PE4_RX_DN1	B6	PE4_TX_DN1
A7	GND	B7	GND
A8	B12_IFDET1_MCIO19	B8	SMB_MCIO19_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO19_SDA1
A10	GND	B10	GND
A11	CLK_MCIO19_DP1	B11	MCIO_19_PERST0_N
A12	CLK_MCIO19_DN1	B12	MCIO_19_PRST0_N
A13	GND	B13	GND
A14	PE4_RX_DP2	B14	PE4_TX_DP2
A15	PE4_RX_DN2	B15	PE4_TX_DN2
A16	GND	B16	GND
A17	PE4_RX_DP3	B17	PE4_TX_DP3
A18	PE4_RX_DN3	B18	PE4_TX_DN3
A19	GND	B19	GND
A20	PE4_RX_DP4	B20	PE4_TX_DP4
A21	PE4_RX_DN4	B21	PE4_TX_DN4
A22	GND	B22	GND
A23	PE4_RX_DP5	B23	PE4_TX_DP5
A24	PE4_RX_DN5	B24	PE4_TX_DN5
A25	GND	B25	GND
A26	B30_IFDET2_MCIO19	B26	SMB_MCIO19_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO19_SDA2
A28	GND	B28	GND
A29	CLK_MCIO19_DP2	B29	MCIO_19_PERST1_N
A30	CLK_MCIO19_DN2	B30	MCIO_19_PRST1_N
A31	GND	B31	GND
A32	PE4_RX_DP6	B32	PE4_TX_DP6
A33	PE4_RX_DN6	B33	PE4_TX_DN6
A34	GND	B34	GND
A35	PE4_RX_DP7	B35	PE4_TX_DP7
A36	PE4_RX_DN7	B36	PE4_TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO20 Pin Definition [CPU1]

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	PE4_RX_DP8	B2	PE4_TX_DP8
A3	PE4_RX_DN8	B3	PE4_TX_DN8
A4	GND	B4	GND
A5	PE4_RX_DP9	B5	PE4_TX_DP9
A6	PE4_RX_DN9	B6	PE4_TX_DN9
A7	GND	B7	GND
A8	B12_IFDET1_MCIO20	B8	SMB_MCIO20_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO20_SDA1
A10	GND	B10	GND
A11	CLK_MCIO20_DP1	B11	MCIO_20_PERST0_N
A12	CLK_MCIO20_DN1	B12	MCIO_20_PRSENT0_N
A13	GND	B13	GND
A14	PE4_RX_DP10	B14	PE4_TX_DP10
A15	PE4_RX_DN10	B15	PE4_TX_DN10
A16	GND	B16	GND
A17	PE4_RX_DP11	B17	PE4_TX_DP11
A18	PE4_RX_DN11	B18	PE4_TX_DN11
A19	GND	B19	GND
A20	PE4_RX_DP12	B20	PE4_TX_DP12
A21	PE4_RX_DN12	B21	PE4_TX_DN12
A22	GND	B22	GND
A23	PE4_RX_DP13	B23	PE4_TX_DP13
A24	PE4_RX_DN13	B24	PE4_TX_DN13
A25	GND	B25	GND
A26	B30_IFDET2_MCIO20	B26	SMB_MCIO20_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO20_SDA2
A28	GND	B28	GND
A29	CLK_MCIO20_DP2	B29	MCIO_20_PERST1_N
A30	CLK_MCIO20_DN2	B30	MCIO_20_PRSENT1_N
A31	GND	B31	GND
A32	PE4_RX_DP14	B32	PE4_TX_DP14
A33	PE4_RX_DN14	B33	PE4_TX_DN14
A34	GND	B34	GND
A35	PE4_RX_DP15	B35	PE4_TX_DP15
A36	PE4_RX_DN15	B36	PE4_TX_DN15
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO21 Pin Definition [CPU1]

Pin	Definition	Pin	Definition
A1	GND	B1	GND
A2	RX_DP0	B2	TX_DP0
A3	RX_DN0	B3	TX_DN0
A4	GND	B4	GND
A5	RX_DP1	B5	TX_DP1
A6	RX_DN1	B6	TX_DN1
A7	GND	B7	GND
A8	B12_IFDET1_MCIO21	B8	SMB_MCIO21_SCL1
A9	WAKE_LVC3_N	B9	SMB_MCIO21_SDA1
A10	GND	B10	GND
A11	CLK_MCIO21_DP1	B11	MCIO_21_PERST0_N
A12	CLK_MCIO21_DN1	B12	MCIO_21_PRST0_N
A13	GND	B13	GND
A14	RX_DP2	B14	TX_DP2
A15	RX_DN2	B15	TX_DN2
A16	GND	B16	GND
A17	RX_DP3	B17	TX_DP3
A18	RX_DN3	B18	TX_DN3
A19	GND	B19	GND
A20	RX_DP4	B20	TX_DP4
A21	RX_DN4	B21	TX_DN4
A22	GND	B22	GND
A23	RX_DP5	B23	TX_DP5
A24	RX_DN5	B24	TX_DN5
A25	GND	B25	GND
A26	B30_IFDET2_MCIO21	B26	SMB_MCIO21_SCL2
A27	WAKE_LVC3_N	B27	SMB_MCIO21_SDA2
A28	GND	B28	GND
A29	CLK_MCIO21_DP2	B29	MCIO_21_PERST1_N
A30	CLK_MCIO21_DN2	B30	MCIO_21_PRST1_N
A31	GND	B31	GND
A32	RX_DP6	B32	TX_DP6
A33	RX_DN6	B33	TX_DN6
A34	GND	B34	GND
A35	RX_DP7	B35	TX_DP7
A36	RX_DN7	B36	TX_DN7
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

2.7 Dr. Debug

Dr. Debug is used to provide code information, which makes troubleshooting even easier. Please see the diagrams below for reading the Dr. Debug codes.

Code	Description
0x10	PEI_CORE_STARTED
0x11	PEI_CAR_CPU_INIT
0x15	PEI_CAR_NB_INIT
0x19	PEI_CAR_SB_INIT
0x31	PEI_MEMORY_INSTALLED
0x32	PEI_CPU_INIT
0x33	PEI_CPU_CACHE_INIT
0x34	PEI_CPU_AP_INIT
0x35	PEI_CPU_BSP_SELECT
0x36	PEI_CPU_SMM_INIT
0x37	PEI_MEM_NB_INIT
0x3B	PEI_MEM_SB_INIT
0x4F	PEI_DXE_IPL_STARTED
0x60	DXE_CORE_STARTED
0x61	DXE_NVRAM_INIT
0x62	DXE_SBRUN_INIT

0x63	DXE_CPU_INIT
0x68	DXE_NB_HB_INIT
0x69	DXE_NB_INIT
0x6A	DXE_NB_SMM_INIT
0x70	DXE_SB_INIT
0x71	DXE_SB_SMM_INIT
0x72	DXE_SB_DEVICES_INIT
0x78	DXE_ACPI_INIT
0x79	DXE_CSM_INIT
0x90	DXE_BDS_STARTED
0x91	DXE_BDS_CONNECT_DRIVERS
0x92	DXE_PCI_BUS_BEGIN
0x93	DXE_PCI_BUS_HPC_INIT
0x94	DXE_PCI_BUS_ENUM
0x95	DXE_PCI_BUS_REQUEST_RESOURCES
0x96	DXE_PCI_BUS_ASSIGN_RESOURCES
0x97	DXE_CON_OUT_CONNECT
0x98	DXE_CON_IN_CONNECT

0x99 DXE_SIO_INIT

0x9A DXE_USB_BEGIN

0x9B DXE_USB_RESET

0x9C DXE_USB_DETECT

0x9D DXE_USB_ENABLE

0xA0 DXE_IDE_BEGIN

0xA1 DXE_IDE_RESET

0xA2 DXE_IDE_DETECT

0xA3 DXE_IDE_ENABLE

0xA4 DXE_SCSI_BEGIN

0xA5 DXE_SCSI_RESET

0xA6 DXE_SCSI_DETECT

0xA7 DXE_SCSI_ENABLE

0xA8 DXE_SETUP_VERIFYING_PASSWORD

0xA9 DXE_SETUP_START

0xAB DXE_SETUP_INPUT_WAIT

0xAD DXE_READY_TO_BOOT

0xAE DXE_LEGACY_BOOT

0xAF	DXE_EXIT_BOOT_SERVICES
0xB0	RT_SET_VIRTUAL_ADDRESS_MAP_BEGIN
0xB1	RT_SET_VIRTUAL_ADDRESS_MAP_END
0xB2	DXE_LEGACY_OPMOM_INIT
0xB3	DXE_RESET_SYSTEM
0xB4	DXE_USB_HOTPLUG
0xB5	DXE_PCI_BUS_HOTPLUG
0xB6	DXE_NVRAM_CLEANUP
0xB7	DXE_CONFIGURATION_RESET
0xF0	PEI_RECOVERY_AUTO
0xF1	PEI_RECOVERY_USER
0xF2	PEI_RECOVERY_STARTED
0xF3	PEI_RECOVERY_CAPSULE_FOUND
0xF4	PEI_RECOVERY_CAPSULE_LOADED
0xE0	PEI_S3_STARTED
0xE1	PEI_S3_BOOT_SCRIPT
0xE2	PEI_S3_VIDEO_REPOST

0xE3 PEI_S3_OS_WAKE

0x50 PEI_MEMORY_INVALID_TYPE

0x53 PEI_MEMORY_NOT_DETECTED

0x55 PEI_MEMORY_NOT_INSTALLED

0x57 PEI_CPU_MISMATCH

0x58 PEI_CPU_SELF_TEST_FAILED

0x59 PEI_CPU_NO_MICROCODE

0x5A PEI_CPU_ERROR

0x5B PEI_RESET_NOT_AVAILABLE

0xD0 DXE_CPU_ERROR

0xD1 DXE_NB_ERROR

0xD2 DXE_SB_ERROR

0xD3 DXE_ARCH_PROTOCOL_NOT_AVAILABLE

0xD4 DXE_PCI_BUS_OUT_OF_RESOURCES

0xD5 DXE_LEGACY_OPROM_NO_SPACE

0xD6 DXE_NO_CON_OUT

0xD7 DXE_NO_CON_IN

0xD8	DXE_INVALID_PASSWORD
0xD9	DXE_BOOT_OPTION_LOAD_ERROR
0xDA	DXE_BOOT_OPTION_FAILED
0xDB	DXE_FLASH_UPDATE_FAILED
0xDC	DXE_RESET_NOT_AVAILABLE
0xE8	PEI_MEMORY_S3_RESUME_FAILED
0xE9	PEI_S3_RESUME_PPI_NOT_FOUND
0xEA	PEI_S3_BOOT_SCRIPT_ERROR
0xEB	PEI_S3_OS_WAKE_ERROR

2.8 Identification purpose LED/Switch

Use the UID button to locate the server working on behind a rack of servers.

Unit Identification
purpose LED/Switch
(UID1)



When the UID button on the front or rear panel is pressed, the front/rear UID blue LED indicator will be truned on. Press the UID button again to turn off the indicator.

Power Switch
(PWR_BTN)



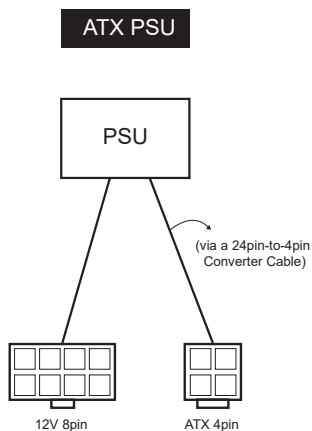
Power Switch allows users to quickly turn on/off the system.



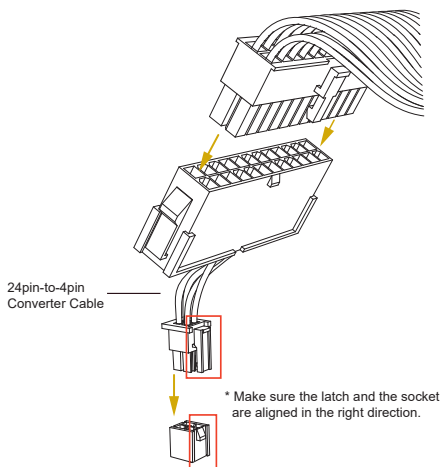
1. Press and hold the UID button for 4 seconds, BMC will trigger an external reset.
2. Press and hold the UID button for 10 seconds, BMC will reset and load default values.

2.9 ATX PSU Power Connections

This motherboard support ATX power input. Please refer to the table below for the required connections between the motherboard and the power supply.



The following diagram illustrates how to connect the bundled ATX 24pin-to-4pin converter cable.



2.10 Dual LAN and Teaming Operation Guide

Dual LAN with Teaming enabled on this motherboard allows two single connections to act as one single connection(s) for twice the transmission bandwidth, making data transmission more effective and improving the quality of transmission of distant images. Fault tolerance on the dual LAN network prevents network downtime by transferring the workload from a failed port to a working port.



The speed of transmission is subject to the actual network environment or status even with Teaming enabled.

Before setting up Teaming, please make sure whether the Switch (or Router) supports Teaming (IEEE 802.3ad Link Aggregation). Specify a preferred adapter in Intel PROSet. Under normal conditions, the Primary adapter handles all non-TCP/IP traffic. The Secondary adapter will receive fallback traffic if the primary fails. If the Preferred Primary adapter fails, but is later restored to an active status, control is automatically switched back to the Preferred Primary adapter.

Step 1

From **Device Manager**, open the properties of a team.

Step 2

Click the **Settings** tab.

Step 3

Click the **Modify Team** button.

Step 4

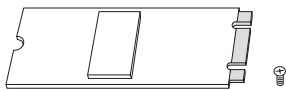
Select the adapter to the primary adapter and click the **Set Primary** button.

If it does not specify a preferred primary adapter, the software will choose an adapter of the highest capability (model and speed) to act as the default primary. If a failover occurs, another adapter becomes the primary. The adapter will, however, rejoin the team as a non-primary.

2.11 M.2 SSD Module Installation Guide

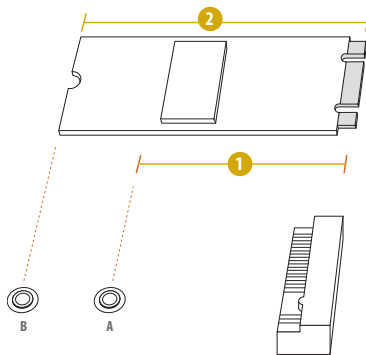
The M.2 Socket (M2_1, Key M) supports type 2280/22110 M.2 PCI Express module up to Gen5 x4 (32GT/s x4).

Installing the M.2 SSD Module



Step 1

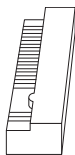
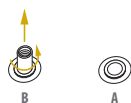
Prepare a M.2 SSD module and the screw.



Step 2

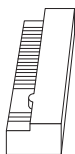
Depending on the PCB type and length of the M.2 SSD module, find the corresponding nut location to be used.

No.	1	2
Nut Location	A (NUT2280_1)	B (NUT22110_1)
PCB Length	8cm	11cm
Module Type	Type 2280	Type 22110



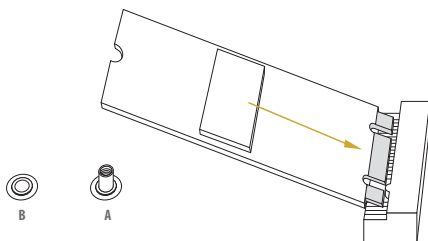
Step 3

Move the standoff based on the module type and length.
Skip Step 3 and 4 and go straight to Step 5 if using the default nut.
Otherwise, release the standoff by hand.



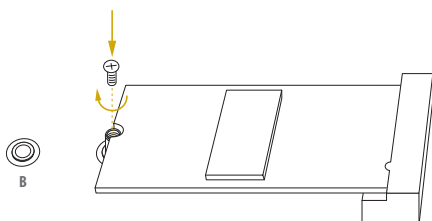
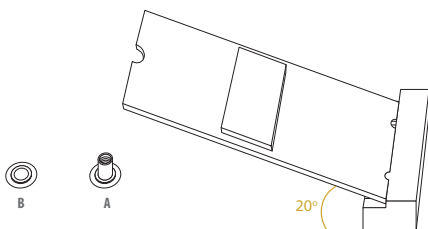
Step 4

Peel off the yellow protective film on the nut to be used. Hand tighten the standoff into the desired nut location on the motherboard.



Step 5

Align and gently insert the M.2 SSD module into the M.2 slot. Please be aware that the M.2 SSD module only fits in one orientation.



Step 6

Tighten the screw with a screwdriver to secure the module into place.
Please do not overtighten the screw as this might damage the module.

Chapter 3 UEFI Setup Utility

3.1 Introduction

This section explains how to use the UEFI SETUP UTILITY to configure the system. The UEFI chip on the motherboard stores the UEFI SETUP UTILITY. Run the UEFI SETUP UTILITY when starting up the computer. Please press <F2> or during the Power-On-Self-Test (POST) to enter the UEFI SETUP UTILITY; otherwise, POST will continue with its test routines.

Restart the system by pressing <Ctrl> + <Alt> + <Delete> to enter the UEFI SETUP UTILITY after POST, or by pressing the reset button on the system chassis. This allows user to restart by turning the system off and then back on.



Because the UEFI software is constantly being updated, the following UEFI setup screens and descriptions are for reference purpose only, and they may not exactly match what seeing on the screen.

3.1.1 UEFI Menu Bar

The top of the screen has a menu bar with the following selections:

Item	Description
Main	To set up the system time/date information
Advanced	To set up the advanced UEFI features
Server Mgmt	To manage the server
Event Logs	For event log configuration
Security	To set up the security features
Boot	To set up the default system device to locate and load the Operating System
Exit	To exit the current screen or the UEFI SETUP UTILITY

Use <←> key or <→> key to choose among the selections on the menu bar, and then press <Enter> to get into the sub screen.

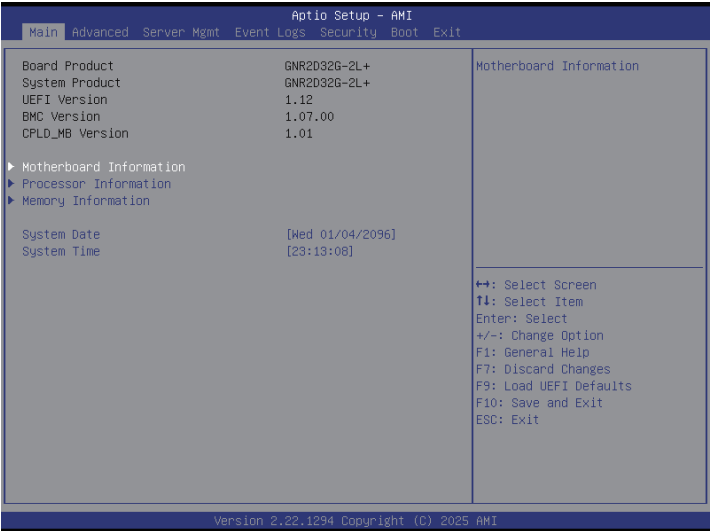
3.1.2 Navigation Keys

Please check the following table for the function description of each navigation key.

Navigation Key(s)	Function Description
← / →	Moves cursor left or right to select Screens
↑ / ↓	Moves cursor up or down to select items
+ / -	To change option for the selected items
<Tab>	Switch to next function
<Enter>	To bring up the selected screen
<PGUP>	Go to the previous page
<PGDN>	Go to the next page
<HOME>	Go to the top of the screen
<END>	Go to the bottom of the screen
<F1>	To display the General Help Screen
<F7>	Discard changes and exit the UEFI SETUP UTILITY
<F9>	Load optimal default values for all the settings
<F10>	Save changes and exit the UEFI SETUP UTILITY
<F12>	Print screen
<ESC>	Jump to the Exit Screen or exit the current screen

3.2 Main Screen

Once entering the UEFI SETUP UTILITY, the Main screen will appear and display the system overview. The Main screen provides system overview information and allows user- to set the system time and date.



The screenshots in this user manual are examples and for references only. The actual images may slightly vary depending on the model and the version used.

3.2.1 Mother Board Information

Press <Enter> to view the information of the motheboard.

Aptio Setup - AMI		
Main		
Motherboard Information		
Motherboard	GNR2D32G-2Lplus	
BIOS Information		
BIOS Vendor	American Megatrends	
Core Version	5.35	
Compliance	UEFI 2.9; PI 1.7	
Project Version	A3259 1.12 x64	
Build Date and Time	02/11/2025 15:30:43	
Intel RC Revision	3544.P29	
AMI RC Revision	0AC02 0.70	
BIOS ACM	1.0.7	
SINIT ACM	1.0.7	
ACPI Version	65	
SMBIOS Version	3.7.0	
Platform Information		
Platform	BeechnutCityRP	
Processor	A06D1 - GNR XCC Bx	
		←+: Select Screen ↑↓: Select Item Enter: Select +/-: Change Option F1: General Help F7: Discard Changes F9: Load UEFI Defaults F10: Save and Exit ESC: Exit
Version 2.22.1294 Copyright (C) 2025 AMI		

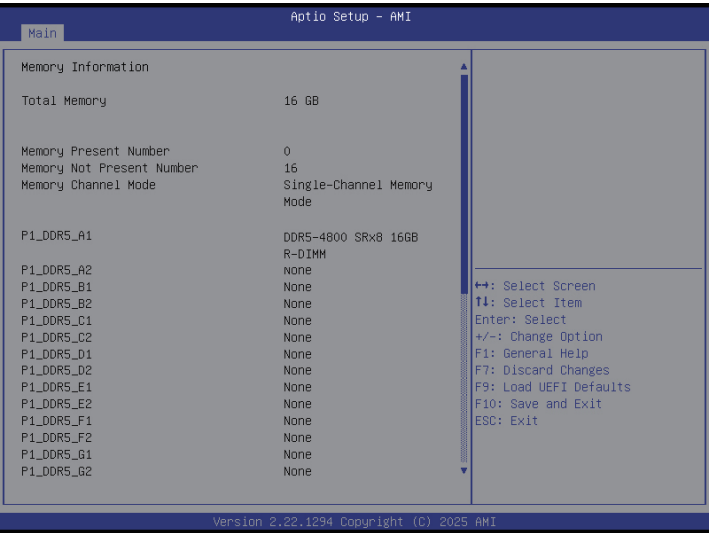
3.2.2 Processor Information

Press <Enter> to view the information of the processor.

Aptio Setup - AMI		
Main		
Processor Information		
Processor BSP Revision	A06D1 - GNR B0	
Processor Socket	CPU1	CPU2
Processor ID	000A06D1	000A06D1
Processor Frequency	2.700GHz	2.700GHz
Processor Core	48-Core	48-Core
Memory Channel	8	8
Processor Max Ratio	1BH	1BH
Processor Min Ratio	08H	08H
Microcode Revision	01000380	01000380
L1 Cache RAM	112KB	112KB
L2 Cache RAM	2048KB	2048KB
L3 Cache RAM	294912KB	294912KB
CPU1 Version	Intel(R) Xeon(R) 6747P	
CPU2 Version	Intel(R) Xeon(R) 6747P	
Intel Turbo Boost	Support	
Intel VT-d Technology	Support	
		←+: Select Screen ↑↓: Select Item Enter: Select +/-: Change Option F1: General Help F7: Discard Changes F9: Load UEFI Defaults F10: Save and Exit ESC: Exit
Version 2.22.1294 Copyright (C) 2025 AMI		

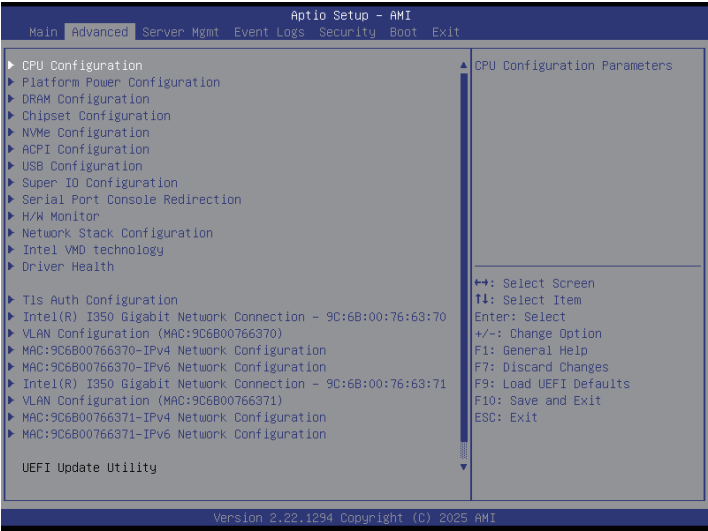
3.2.3 Memory Information

Press <Enter> to view the information of the memory.



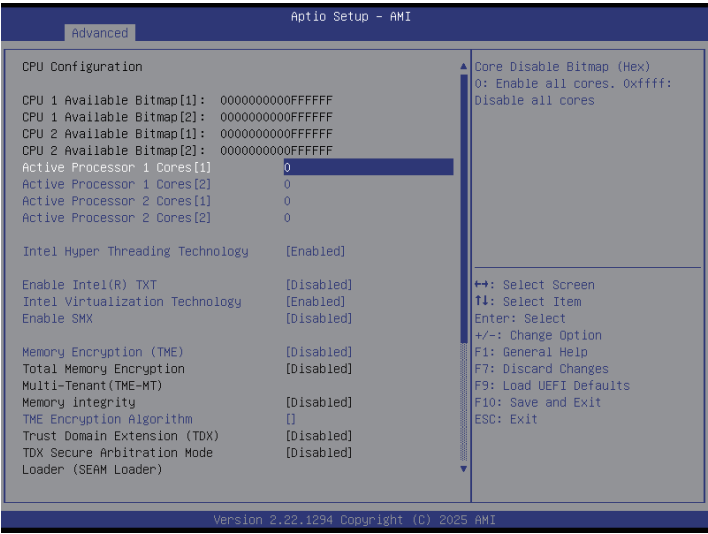
3.3 Advanced Screen

In this section, set the configurations for the following items: CPU Configuration, Platform Power Configuration, DRAM Configuration, Chipset Configuration, NVMe Configuration, ACPI Configuration, USB Configuration, Super IO Configuration, Serial Port Console Redirection, H/W Monitor, Network Stack Configuration, Intel VMD Technology, Driver Health, Tls Auth Configuration, Intel(R) Network Connection, VLAN Configuration, and Instant Flash.



Setting wrong values in this section may cause the system to malfunction.

3.3.1 CPU Configuration



Active Processor 1 Cores [1]/[2]

Core Disable Bitmap (Hex)

0: Enable all cores.

0xffff: Didable all cores.

Active Processor 2 Cores [1]/[2]

Core Disable Bitmap (Hex)

0: Enable all cores.

0xffff: Didable all cores.

Intel Hyper Threading Technology

Intel Hyper Threading Technology allows multiple threads to run on each core, so that the overall performance on threaded software is improved.

Enable Intel(R) TXT

Enables Intel Trusted Execution Technology Configuration.

Intel Virtualization Technology

Intel Virtualization Technology allows a platform to run multiple operating systems and applications in independent partitions, so that one computer system can function as multiple virtual systems.

Enable SMX

Use this item to enable Safer Mode Extensions.

Memory Encryption (TME)

Use this item to enable or disable Memory Encryption (TME).

Total Memory Encryption Multi-Tenant (TME-MT)

Use this item to enable or disable Total Memory Encryption-Multi-Tenant (TME-MT).
Can be enabled only if Socket Configuration -> Porcessor Configuration -> Limit CPU PA to 46 bits=Disable.

Memory Integrity

Use this item to enable or disable memory Integrity.

TME Encryption Algorithm

Use this item to select TME Encryption Algorithm.

Trust Domain Extension (TDX)

Use this item to enable or disable Trust Domain Extension (TDX).

TDX Secure Arbitration Mode Loader (SEAM Loader)

Use this item to enable or disable TDX Secure Arbitration Mode Loader (SEAM Loader).

TME-MT/TDX key split

Designate number of bits for TDX usage. The rest will be used by TME-MT.

SGX Factory Reset

Perform SGX Factory Reset, on subsequent boot: delete all registration data, if SGX enabled will force Initial Platform Establishment flow.

SW Guard Extensions (SGX)

Use this item to enable or disable Software Guard Extensions (SGX).

SGX PRMRR Size Requested

Use this item to select the SGX PRMRR Size per domain.

SGX QoS

Use this item to enable or disable SGX Quality of Service.

Select Owner EPOCH input type

Each EPOCH is 64bit, keys value should be different than 0. After generating new epoch via 'Change to New Random Owner EPOCHs', the selection reverts back to 'Manual User Defined Owner EPOCHs'. In next boot keys will be hidden and state will be 'SGX Owner EPOCH activated'.

SGX Registration Server

Use this item to choose which server should be used for SGX registration.

Disable ACTM Launch

Use this item to disable ACTM Launch.

DCU Streamer Prefetcher

DCU streamer prefetcher is an L1 data cache prefetcher (MSR 1A4h [2])

Hardware Prefetcher

Automatically prefetch data and code for the processor. Enable for better performance.

Adjacent Cache Line Prefetch

Automatically prefetch the subsequent cache line while retrieving the currently requested cache line. Enable for better performance.

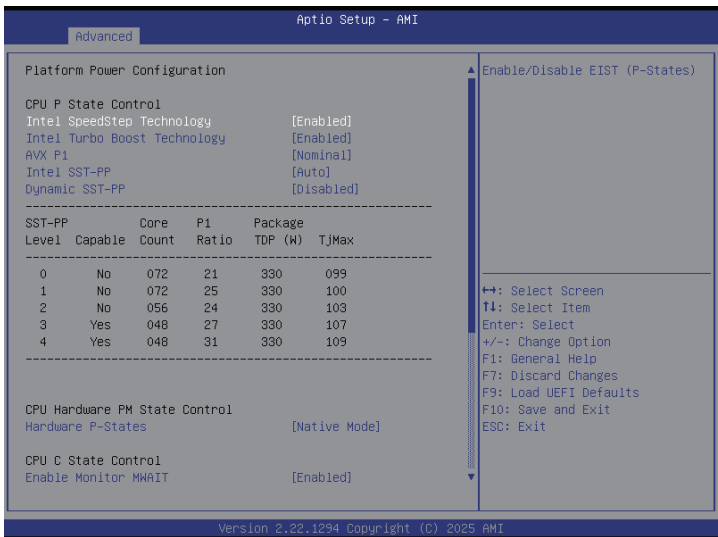
AES-NI

Use this item to enable or disable AES-NI support.

SNC

Use this item to enable or disable SNC mode. Configure this item to Disable, BIOS will enable UMA mode. Number of clusters is determined by BIOS based on detected SKU.

3.3.2 Platform Power Configuration



Intel SpeedStep Technology

Intel SpeedStep technology allows processors to switch between multiple frequencies and voltage points for better power saving and heat dissipation. CPU turbo ratio can be fixed when Intel SpeedStep Technology set Disabled and Intel Turbo Boost Technology set Enabled.



Please note that enabling this function may reduce CPU voltage and lead to system stability or compatibility issues with some power supplies. Please set this item to [Disabled] if above issues occur.

Intel Turbo Boost Technology

Intel Turbo Boost Technology enables the processor to run above its base operating frequency when the operating system requests the highest performance state.

AVX P1

Use this item to select AVX P1 level.

Intel SST-PP

Intel SST-PP Select allows user to choose level. Auto: Choose the lowest level hardware support.

Dynamic SST-PP

Use this item to enable or disable the Dynamic SST-PP.



HWP Native Mode is a pre-requisite for enabling Dynamic SST-PP.

Hardware P-States

This item supports below selections:

Disable: Hardware chooses a P-state based on OS Request (Legacy P-States).

Native Mode: Hardware chooses a P-state based on OS guidance.

Out of Band Mode: Hardware autonomously chooses a P-state (no OS guidance)

Native Mode with No Legacy Support: Hardware autonomously chooses a P-state based on OS guidance with no legacy support.

Enable Monitor MWAIT

Use this item to configure Monitor and MWAIT instructions whether Auto maps to enable.

ACPI C6x Enumeration

Auto: Maps to C6-P as ACPI C2.

Disable: Don't enumerate any C6 state in ACPI

C6 as ACPI C2/C3: Enumerate C6 as ACPI C2/C3 state. PkgC6 is not allowed.

C6-P as ACPI C2/C3: Enumerate C6-P as ACPI C2/C3 state. PkgC6 is allowed.

C1 to Cle Promotion

CPU will promote C1 request to Cle state.

Package C State

Package C State limit, the state Auto maps is program specific.

Power Performance Tuning

Use this item to decides which controls EFB.

OS Controls EPB: Specifies IA32_ENERGY_PERF_BIAS is used.

BIOS Controls EPB: Specifies ENERGY_PERF_BIAS_CONFIG is used.

PECI Controls EPB: Specifies PCS53 is used.

ENERGY_PERF_BIAS_CFG mode

Use this item to use input from ENERGY_PERF_BIAS_CONFIG mode selection. PERF/Balanced, Perf/Balanced or Power/Power.

PL1 Power Limit

Use this item to configure Package Power Limit 1 (PL1) in watts. PL1 Power Limit is in Watts and the value may vary from 0 to Fused Value. If the value is 0, the fused value will be programmed. A value greater than fused TDP value will not be programmed.

PL1 Time Window

PL1 value in seconds. The value may vary from 1 to 5. Indicates the time window over which TDP value should be maintained.

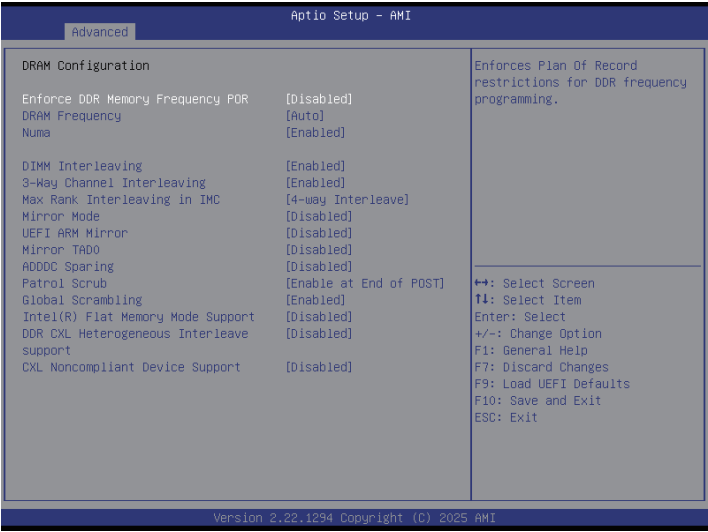
PL2 Power Limit

PL2 Power Limit in Watts. The value may vary from 0 to 120% Fused TDP Value. If the value is 0, BIOS programs $120\% * \text{Fused TDP value}$.

PL2 Time Window

PL2 value in seconds. The value may vary from 0.012 to 0.039. Indicates the time window over which TDP value should be maintained.

3.3.3 DRAM Configuration



Enforce DDR Memory Frequency POR

Select this time to enable or disable the Enforces Plan of Record restrictions for DDR frequency programming.

DRAM Frequency

Maximum Host DDR Memory Frequency Selections in MT/s. If the "AUTO" option has been selected, a frequency is chosen automatically based on the minimum tCK given by the SPD. If Enforce POR is disabled, user will be able to run at higher frequencies than the memory support (limited by processor support).

Numa

Use this item to enable or disable Non Uniform Memory Access (NUMA).

DIMM Interleaving

Enable this item to allow interleaving to be performed at the highest possible MC * Channel interleaving ways or disable it to enforce interleaving to only 1-way.

3-Way Channel Interleaving

Enable this item to allow 3-way channel interleaving or disable it to default to number of channels available per MC when DIMM interleaving is enabled.

Max Rank Interleaving in IMC

Use this item to configure the rank interleaving settings.

Mirror Mode

Full Mirror Mode will set entire ILM memory in system to be mirrored, consequently reducing the memory capacity by half. Partial Mirror Mode will enable the required size of memory to be mirrored. If rank sparing is enabled partial mirroring will not take effect. Enabling any type of Mirror Mode will disable XPT Prefetch.

UEFI ARM Mirror

Imitate behavior of UEFI based Address Range Mirror with setup option.

Mirror TAD0

Enable Mirror on entire memory for TAD0.

ARM Mirror Percentage

Enter the percentage to be mirrored in basis points. Mirror options are 10%, 15%, 20%, 25%, 30%, 35%, 40%. 25% is represented 2500. Any other number entered will be rounded to nearest greater number, for ex. number > 2000 and <=2500 will be rounded to 2500. And any number >4000, will be rounded to 4000.

ADDDC Sparing

Enable or disable Memory Rank Sparing.

Patrol Scrub

Patrol Scrub is a background activity initiated by the processor to seek out and fix memory errors. The default value is [Enabled].

Global Scrambling

Enable - Enables global data scrambling.

Disable - Disables this feature.

Intel(R) Flat Memory Mode Support

Enable or disable Intel(R) Flat Memory Mode support.

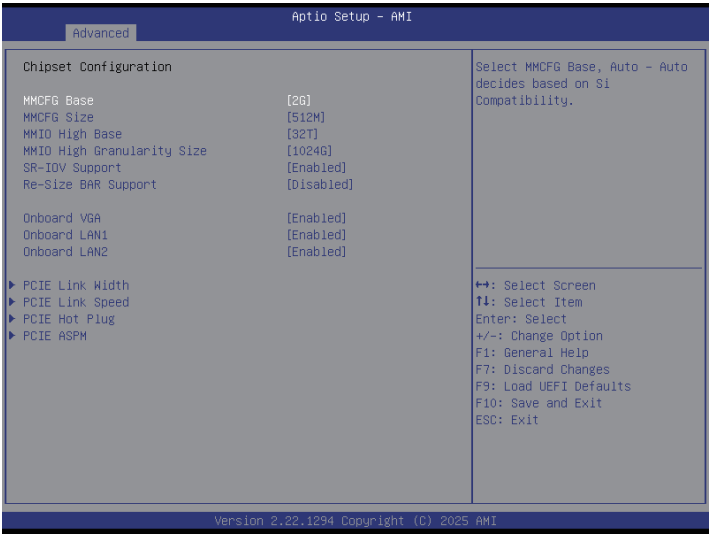
DDR CXL Heterogeneous Interleave support

Use this item to enable DDR CXL Heterogeneous Interleave support.

CXL Noncompliant Device Support

Enables DDR CXL Heterogeneous Interleave support.

3.3.4 Chipset Configuration



MMCFG Base

Use this item to select MMCFG Base. Auto-Auto decides based on Si compatibility.

MMCFG Size

Use this item to select MMCFG Size. Auto-Auto decides based on Si compatibility.

MMIO High Base

Use this item to select MMIO High Base.

MMIO High Granularity Size

Selects the allocation size used to assign mmioh resources. Per stack mmioh resource assignments are multiples of the granularity where 1 unit per stack is the default allocation.

SR-IOV Support

If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.

Re-Sized BAR Support

If system has Resizable BAR capable PCIe Devices, this option Enables or Disables Resizable BAR Support.

Onboard VGA

Use this to enable or disable the Onboard VGA function.

Onboard LAN1/LAN2

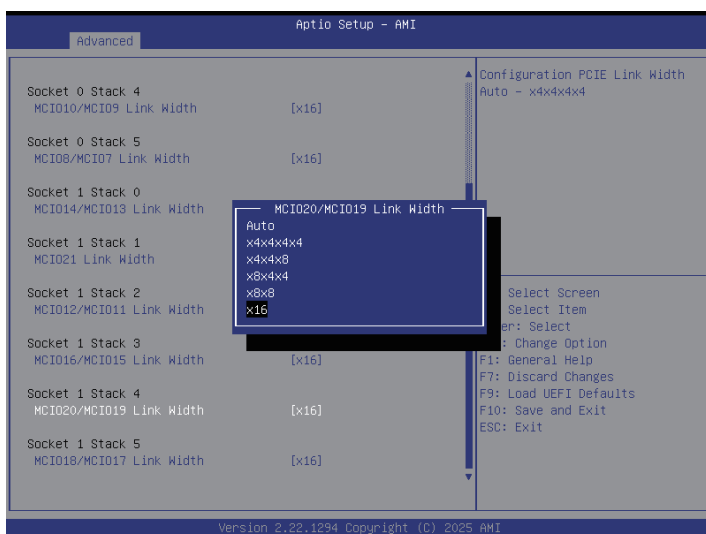
Use this item to enable or disable the Boot From Onboard LAN feature.

PCIE Link Width

This displays the PCIE Link Width.

**MCIO1/MCIO2/MCIO3/MCIO4/MCIO5/MCIO6/MCIO7/MCIO8/
MCIO9/MCIO10/MCIO11/MCIO12/MCIO13/MCIO14/MCIO15/
MCIO16/MCIO17/MCIO18/MCIO19/MCIO20/MCIO21 Link Width**

The default value for MCIO21 is [x4x4], others are [x16].



PCIE Link Speed

This displays the PCIE Link Speed.

**MCIO1/MCIO2/MCIO3/MCIO4/MCIO5/MCIO6/MCIO7/MCIO8/MCIO9/
MCIO10/MCIO11/MCIO12/MCIO13/MCIO14/MCIO15/MCIO16/MCIO17/
MCIO18/MCIO19/MCIO20/MCIO21-1/MCIO21-2 Link Speed**

The default value is [Auto] - up to Gen5 (32GT/s).

M2_1 Link Speed

The default value is [Auto] - up to Gen5 (32GT/s).

PCIE Hot Plug

Select this item to configure PCIE Hot Plug.

**MCIO1/MCIO2/MCIO3/MCIO4/MCIO5/MCIO6/MCIO7/MCIO8/MCIO9/
MCIO10/MCIO11/MCIO12/MCIO13/MCIO14/MCIO15/MCIO16/MCIO17/
MCIO18/MCIO19/MCIO20/MCIO21-1/MCIO21-2 Surprise Hot Plug**

This option specifies if the link is considered Surprise Hot Plug capable.

PCIE ASPM

Select this item to disable ASPM support in all PCIe root ports.

**MCIO1/MCIO2/MCIO3/MCIO4/MCIO5/MCIO6/MCIO7/MCIO8/MCIO9/
MCIO10/MCIO11/MCIO12/MCIO13/MCIO14/MCIO15/MCIO16/MCIO17/
MCIO18/MCIO19/MCIO20/MCIO21-1/MCIO21-2 ASPM Support**

Use this item to disable ASPM support in PCIe root port. The default value is [Auto].

M2_1 ASPM Support

Use this item to disable ASPM support in PCIe root port. The default value is [Auto].

3.3.5 NVMe Configuration

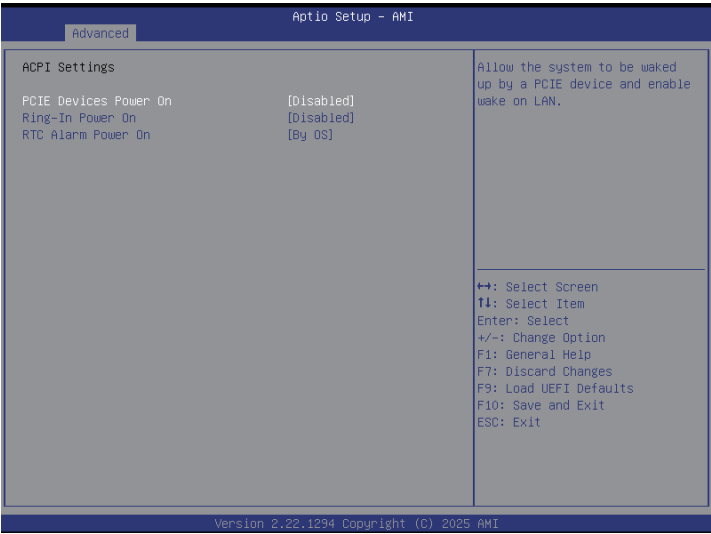


The NVMe Configuration displays the NVMe Drive Options Settings.

Launch NVMe driver

Select this item to enable or disable launch NVMe driver.

3.3.6 ACPI Configuration



PCIE Devices Power On

Allow the system to be waked up by a PCIE device and enable wake on LAN.

Ring-In Power On

Allow the system to be waked up by onboard COM port modem Ring-In Singals.

RTC Alarm Power On

Allow the system to be waked up by real time clock alarm. Set it to By OS to let it be handled by the operating system.

RTC Alarm Date

Use this item to set Date of RTC power on feature.

RTC Alarm Hour

Use this item to set Hour of RTC power on feature.

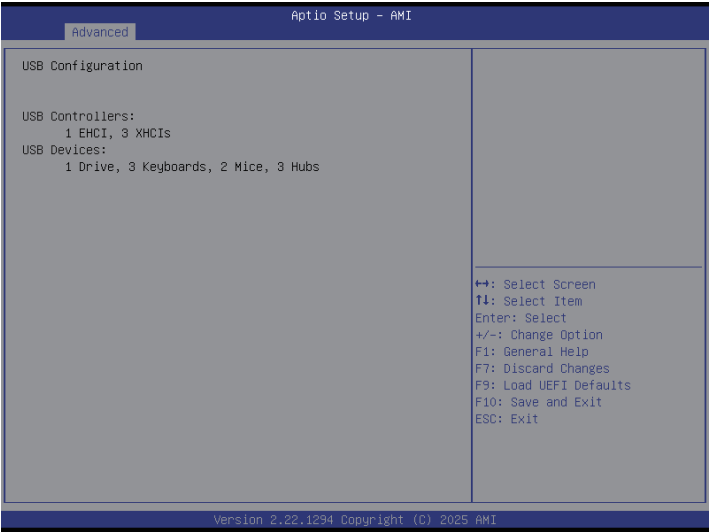
RTC Alarm Minute

Use this item to set Minute of RTC power on feature.

RTC Alarm Second

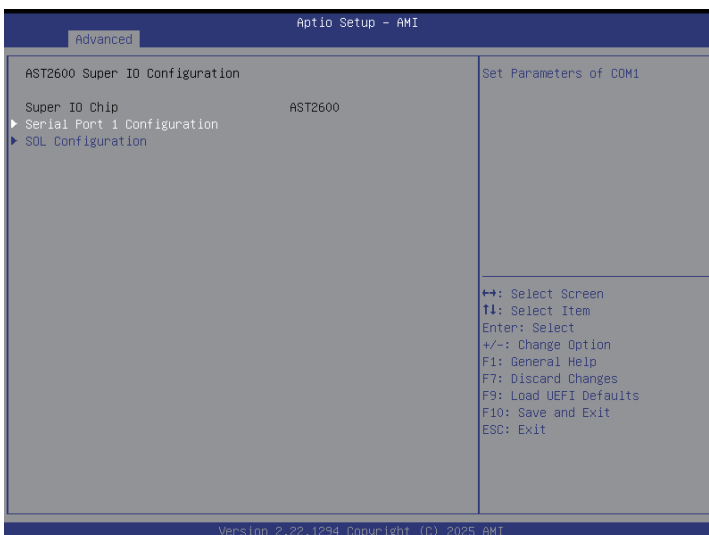
Use this item to set Second of RTC power on feature.

3.3.7 USB Configuration



This displays the USB Module Version, Controllers and USB Devices information.

3.3.8 Super IO Configuration



Serial Port 1 Configuration

Use this item to set parameters of Serial Port 1 (COMA).

Serial Port

Use this item to enable or disable the Serial Port (COM).

Change Settings

Use this item to select an optimal setting for Super IO device.

SOL Configuration

Use this item to set parameters of Serial Port 2 (COMB).

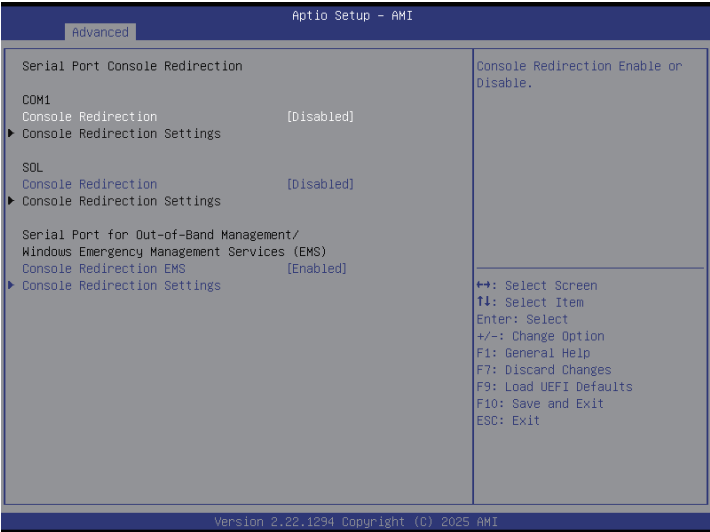
SOL Port

Use this item to enable or disable the Serial Port (COM).

Change Settings

Use this item to select an optimal setting for Super IO device.

3.3.9 Serial Port Console Redirection



COM1 / SOL

Console Redirection

Use this option to enable or disable Console Redirection. If this item is set to Enabled, user can select a COM Port to be used for Console Redirection.

Console Redirection Settings

Use this option to configure Console Redirection Settings, and specify how the computer and the host computer to which are connected exchange information. Both computers should have the same or compatible settings.

Terminal Type

Use this item to select the preferred terminal emulation type for out-of-band management. It is recommended to select [VT-UTF8].

Option	Description
VT100	ASCII character set
VT100Plus	Extended VT100 that supports color and function keys
VT-UTF8	UTF8 encoding is used to map Unicode chars onto 1 or more bytes
ANSI	Extended ASCII character set

Bits Per Second

Use this item to select the serial port transmission speed. The speed used in the host computer and the client computer must be the same. Long or noisy lines may require lower transmission speed. The options include [9600], [19200], [38400], [57600] and [115200].

Data Bits

Use this item to set the data transmission size. The options include [7] and [8] (Bits).

Parity

Use this item to select the parity bit. The options include [None], [Even], [Odd], [Mark] and [Space].

Stop Bits

The item indicates the end of a serial data packet. The standard setting is [1] Stop Bit. Select [2] Stop Bits for slower devices.

Flow Control

Use this item to set the flow control to prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a "stop" signal can be sent to stop the data flow. Once the buffers are empty, a "start" signal can be sent to restart the flow. Hardware flow uses two wires to send start/stop signals. The options include [None] and [Hardware RTS/CTS].

VT-UTF8 Combo Key Support

Use this item to enable or disable the VT-UTF8 Combo Key Support for ANSI/VT100 terminals.

Recorder Mode

Use this item to enable or disable Recorder Mode to capture terminal data and send it as text messages.

Resolution 100x31

Use this item to enable or disable extended terminal resolution support.

Putty Keypad

Use this item to select Function Key and Keypad on Putty.

Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS)**Console Redirection EMS**

Use this option to enable or disable Console Redirection EMS. If this item is set to Enabled, user can select a COM Port to be used for Console Redirection.

Console Redirection Settings

Use this option to configure Console Redirection Settings, and specify how the computer and the host computer to which are connected exchange information.

Out-of-Band Mgmt Port

Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.

Terminal Type EMS

Use this item to select the preferred terminal emulation type for out-of-band management. It is recommended to select [VT-UTF8].

Option	Description
VT100	ASCII character set
VT100+	Extended VT100 that supports color and function keys
VT-UTF8	UTF8 encoding is used to map Unicode chars onto 1 or more bytes
ANSI	Extended ASCII character set

Bits Per Second EMS

Use this item to select the serial port transmission speed. The speed used in the host computer and the client computer must be the same. Long or noisy lines may require lower transmission speed. The options include [9600], [19200], [57600] and [115200].

Flow Control EMS

Use this item to set the flow control to prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a "stop" signal can be sent to stop the data flow. Once the buffers are empty, a "start" signal can be sent to restart the flow. Hardware flow uses two wires to send start/stop signals. The options include [None], [Hardware RTS/CTS], and [Software Xon/Xoff].

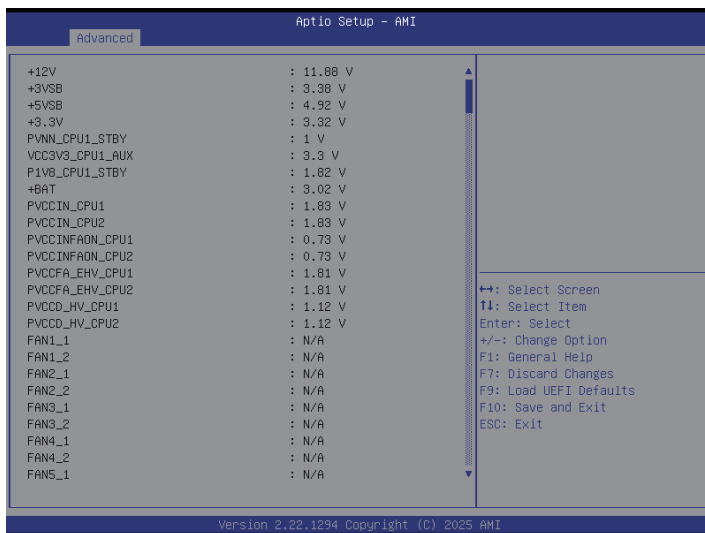
Data Bits EMS

Parity EMS

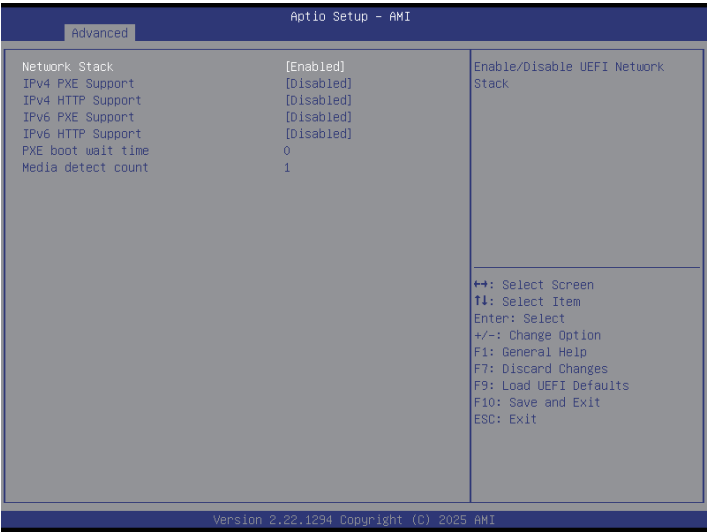
Stop Bits EMS

3.3.10 H/W Monitor

In this section, it allows user to monitor the status of the hardware on the system, including the parameters of the CPU temperature, motherboard temperature, CPU fan speed, chassis fan speed, and the critical voltage.



3.3.11 Network Stack Configuration



Network Stack

Use this to enable or disable UEFI Network Stack.

IPv4 PXE Support

Use this to enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

IPv4 HTTP Support

Use this to enable or disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.

IPv6 PXE Support

Use this to enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

IPv6 HTTP Support

Use this to enable or disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.

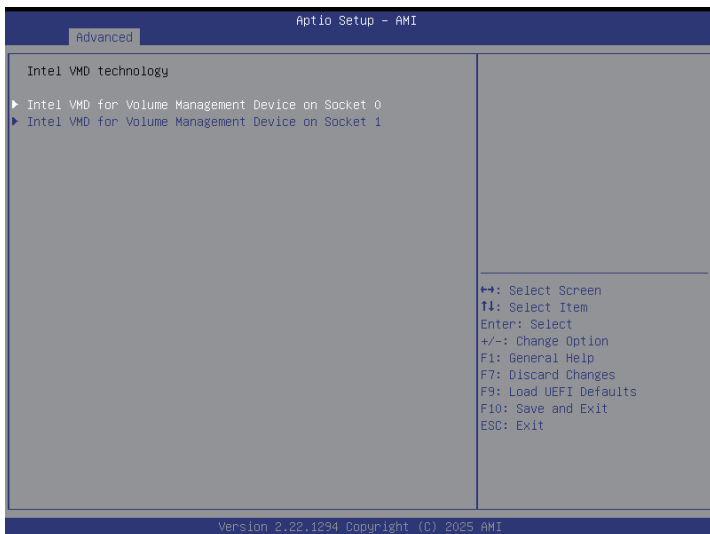
PXE boot wait time

Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

3.3.12 Intel VMD Technology



Press <Enter> to bring up the Intel VMD for Volume Management Device Configuration menu.

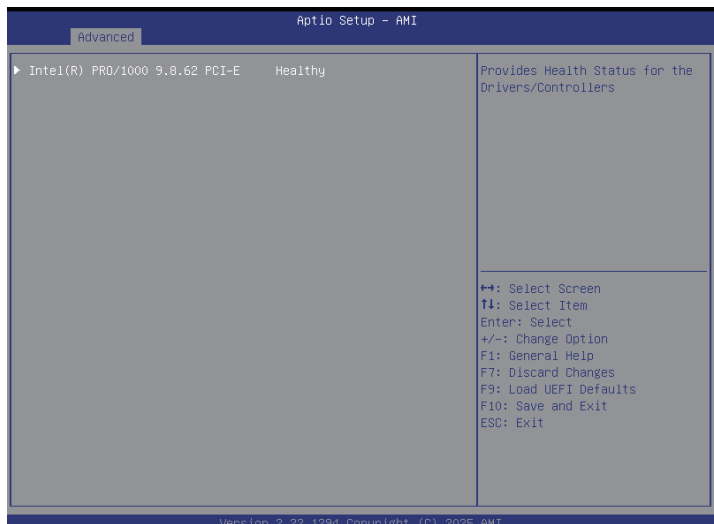
Intel VMD for Volume Management Device on Socket 0/1

VMD Config for Stack 0 (MCIO4/MCIO3)/Stack 1 (M2_1)/Stack 2 (MCIO2/MCIO1)/Stack 3 (MCIO6/MCIO5)/Stack 4 (MCIO10/MCIO9)/Stack 5 (MCIO8/MCIO7)

Use this item to enable or disable Intel Volume Management Device Technology in this Stack.

When [Enabled] allowing user to configure the VMD ports.

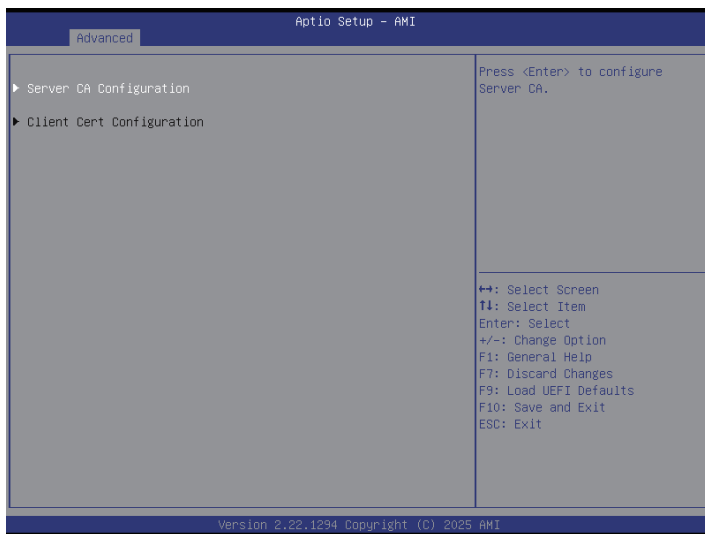
3.3.13 Driver Health



Inter (R) PRO/1000 9.8.62 PCI-E Healthy

Provides Health Status for the Drivers/Controllers

3.3.14 Tls Auth Configuration



Server CA Configuration

Press <Enter> to configure Server CA.

Client Cert Configuration

Enroll Cert

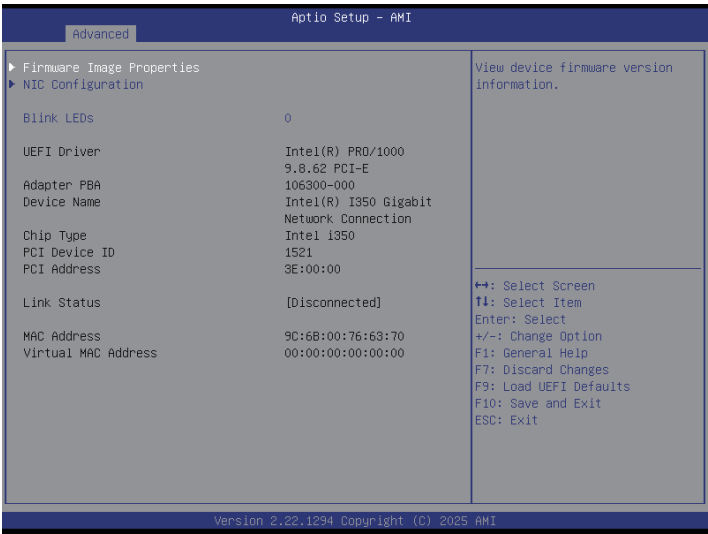
Press <Enter> to enroll cert.

Delete Cert

Press <Enter> to delete cert.

3.3.15 Intel(R) Network Connection

Configure Gigabit Ethernet device parameters.



Firmware Image Properties

Select this item to view the device firmware version information.

NIC Configuration

Click this item to configure the network device port.

Link Speed

Specifies the port speed used for the selected boot protocol.

Wake On LAN

Use this item to enable power on of the system via LAN. Note that configuring Wake on LAN in the operating system does not change the value of this setting, but does override the behavior of Wake on LAN in OS controlled power states.

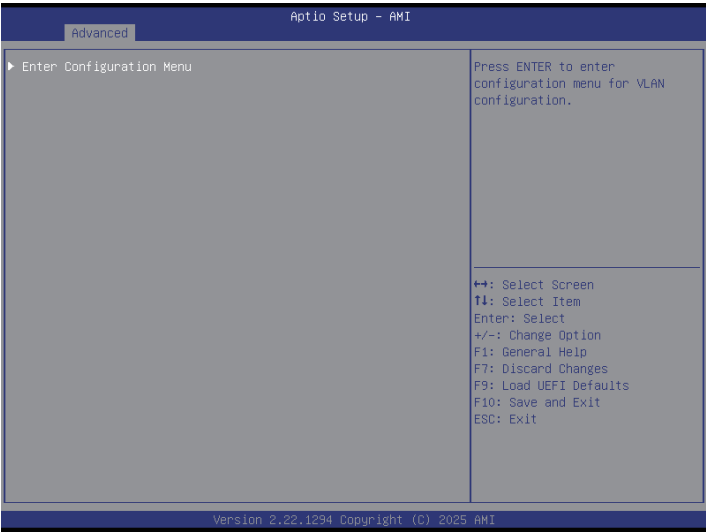
Blink LEDs

Identify the physical network port by blinking the associated LED.

Port Configuration Information

Displays port configuration information including UEFI Driver, Adapter PBA, Device Name, Chip Type, PCI Device ID, PCI Address, Link Status, MAC Address and Virtual MAC Address.

3.3.16 VLAN Configuration



Enter Configuration Menu

Press [Enter] to enter the menu for VLAN configuration.

VLAN ID

Specifies the VLAN ID of new VLAN or existing VLAN, the valid value is 0~4094.

Priority

Specifies the 802.1Q Priority, the valid value is 0~7.

Add VLAN

Use this item to create a new VLAN or update existing VLAN.

Remove VLAN

Use this item to remove selected VLANS.

3.3.17 Instant Flash

Instant Flash is a UEFI flash utility embedded in Flash ROM. This convenient UEFI updatetool allows user to update system UEFI without entering operating systems first like MSDOS or Windows®. Just save the new UEFI file to the USB flash drive, floppy disk or hard drive and launch this tool, then update the UEFI only in a few clicks without preparing an additional floppy diskette or other complicated flash utility. Please be noted that the USB flash drive or hard drive must use FAT32/16/12 file system. Execute the Instant Flash utility, the utility will show the UEFI files and the respective information. Select the proper UEFI file to update UEFI, and reboot the system after the UEFI update process is completed.

3.4 Server Mgmt



Wait For BMC

Wait For BMC response for specified time out. BMC starts at the same time when BIOS starts during AC power ON. It takes around 255 seconds to initialize Host to BMC interfaces.

FRB-2 Timer

Use this item to enable or disable FRB-2 timer (POST timer)

FRB-2 Timer Timeout

Use this to define the FRB-2 Time Expiration between 1 to 30 value.

FRB-2 Timer Policy

Configure how the system should respond. If the FRB-2 Timer expires is disabled, this item is not available.

OS Watchdog Timer

Use this item to enable or disable OS Watchdog Timer. If enabled, starts a BIOS timer which can only be shut off by Management Software after the OS loads.

OS Wtd Timer Timeout

Configure the OS Boot Watchdog Timer Expiration between 1 to 30 min value. If the OS Boot Watchdog Timer is disabled, this item is not available.

OS Wtd Timer Policy

Configure how the system should respond if the OS Boot Watchdog Timer expires. If the OS Boot Watchdog Timer is disabled, this item is not available.

BMC Network Configuration

Use this to configure BMC network parameters.

DNS Configuration

Use this to configure DNS parameters.

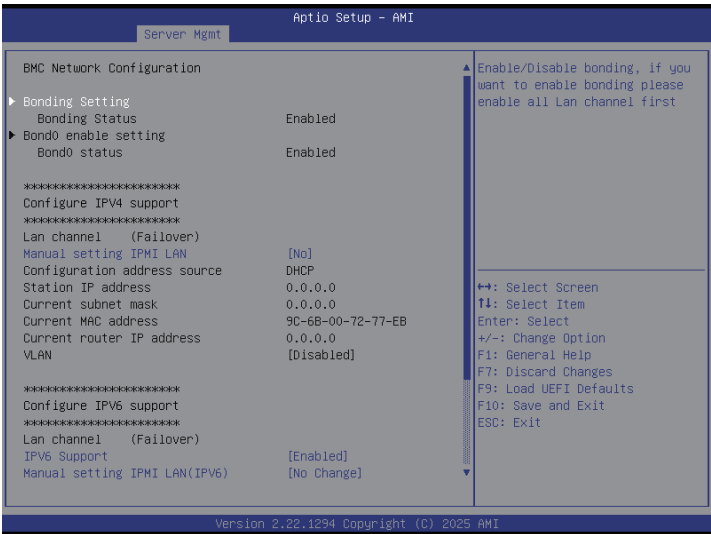
System Event Log

Press <Enter> to change the SEL event log configuration.

BMC Tools

Use this item to configure about KCS control, restore AC power loss and load BMC default settings.

3.4.1 BMC Network Configuration



Bonding Setting

Select this item to enabled or disabled bonding. Please enable all lan channel first when want to enable bonding.

Manual Setting IPMI LAN

If [No] is selected, the IP address is assigned by DHCP. If using a static IP address, toggle to [Yes], and the changes take effect after the system reboots. The default value is [No].

Configuration Address Source

Select to configure BMC network parameters statically or dynamically(by BIOS or BMC). Configuration options: [Static] and [DHCP].

Static: Manually enter the IP Address, Subnet Mask and Gateway Address in the BIOS for BMC LAN channel configuration.

DHCP: IP address, Subnet Mask and Gateway Address are automatically assigned by the network's DHCP server.



The default login information for the IPMI web interface is:

Username: admin

Password: admin

For more instructions on how to set up remote control environment and use the IPMI management platform, please refer to the IPMI Configuration User Guide or go to the Support website at: <http://www.asrockrack.com/support/faq.asp>

VLAN

Enable or disable Virtual Local Area Network.

If [Enabled] is selected, configure the items below.

VLAN ID: Select this item to configure the VLAN ID setting, the Maximum value is 4094 and the Minimum value is 1.

VLAN Priority: Select this item to configure the VLAN Priority setting, the Maximum value is 7 and the Minimum value is 0.

IPv6 Support

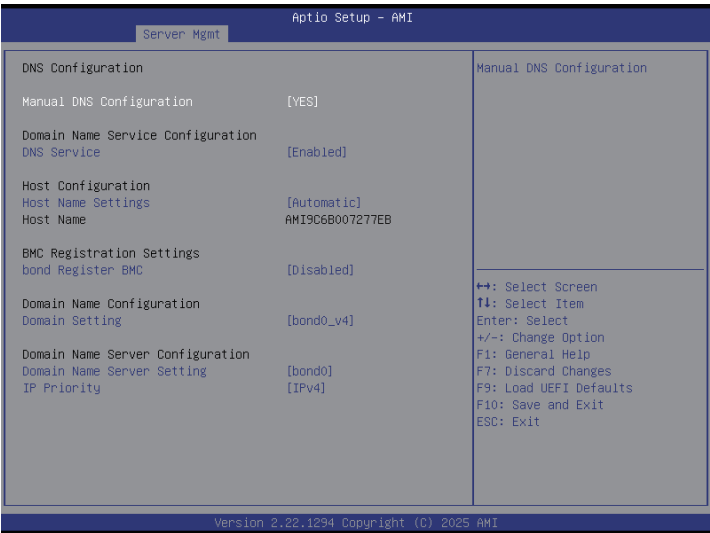
Enable or disable LAN IPv6 Support.

Manual Setting IPMI LAN(IPV6)

Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC).

Unspecified option will not modify any BMC network parameters during BIOS phase.

3.4.2 DNS Configuration



Manual DNS Configuration

Select this item to manual configure DNS.

If [YES] is selected, configure the items below.

DNS Service

Select this item to enable or disable DNS Service Configuration.

Host Name Settings

Select this item to automatic or manual Host Name Settings.

Bond Register BMC

Use this item to enable or disable Bond Register BMC.

Bond Register Method

Use this item to configure Bond Register Method with Nupdate or DHCP client FQDN/Hostname..

Domain Setting

This item supports Manual, Bond0_v4 and Bond0_v6 Domain Settings.

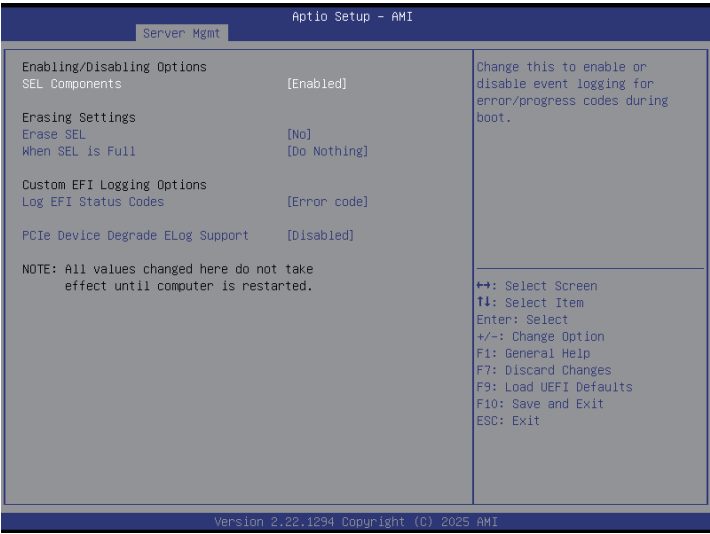
Domain Name Server Setting

Select this item to configure DNS Server Settings.

IP Priority

Select this item to configure IP Priority.

3.4.3 System Event Log



SEL Components

Change this to enable or disable event logging for error/progress codes during boot.

Erase SEL

Use this to choose options for erasing SEL.

When SEL is Full

Use this to choose options for reactions to a full SEL.

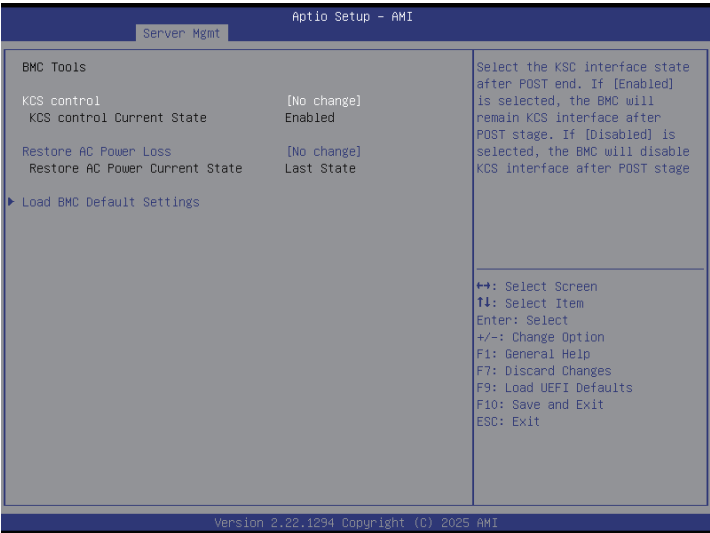
Log EFI Status Codes

Use this item to disable the logging of EFI Status Codes or log only error code or only progress code or both.

PCIe Device Degrade ELog Support

Use this item to enable or disable PCIe Device Degrade Error Logging Support.

3.4.4 BMC Tools



KCS Control

Select this KCS interface state after POST end. If [Enabled] us selected, the BMC will remain KCS interface after POST stage. If [Disabled] is selected, the BMC will disable KCS interface after POST stage

Restore AC Power Loss

This allows user to set the power state after an unexpected AC/power loss. If [Power Off] is selected, the AC/power remains off when the power recovers. If [Power On] is selected, the AC/power resumes and the system starts to boot up when the power recovers. If [Last State] is selected, it will recover to the state before AC/power loss.

Load BMC Default Settings

Use this item to Load BMC Default Settings

3.5 Event Logs



Change Smbios Event Log Settings

Use this item to configure the Smbios Event Log Settings.

When entering the item, the screen displays following sub-items:

Smbios Event Log

Use this item to enable or disable all features of the SMBIOS Event Logging during system boot.

Erase Event Log

Choose options for erasing Smbios Event Log. Erasing is done prior to any logging activation during reset.

When Log is Full

Use this item to choose options for reactions to a full Smbios Event Log. The options include [Do Nothing] and [Erase Immediately].

Log System Boot Event

Choose option to enable/disable logging of System boot event.

View Smbios Event Log

Press <Enter> to view the Smbios Event Log records.



All values changed here do not take effect until computer is restarted.

3.6 Security

This section allows user to set or change the supervisor/user password for the system. For the user password item is allowed user to clear it.



Supervisor Password

Set or change the password for the administrator account. Only the administrator has authority to change the settings in the UEFI Setup Utility. Leave it blank and press enter to remove the password.

User Password

Set or change the password for the user account. Users are unable to change the settings in the UEFI Setup Utility. Leave it blank and press enter to remove the password.

Secure Boot

Select this item to configure the Secure Boot.

Secure Boot

Select this item to enable to support Windows Server 2012 R2 or later versions Secure Boot.

Secure Boot Mode

Secure Boot mode selector: Standard/Custom. In Custom mode, Secure Boot Variables can be configured without authentication.

Install Default Secure Boot Keys

Please install default secure boot keys if it's the first time using secure boot.

Clear Secure Boot Keys

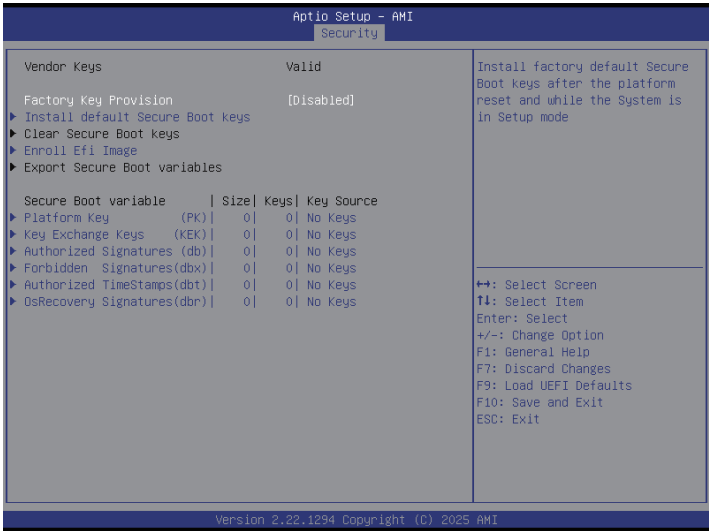
Use this to clear the secure boot keys.

Expert Key Management

Enables expert users to modify Secure Boot Policy variables without variable authentication.

3.6.1 Expert Key Management

In this section, expert users can modify Secure Boot Policy variables without variable authentication.



Factory Key Provision

Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode.

Install Default Secure Boot Keys

Please install default secure boot keys if it's the first time to use secure boot.

Clear Secure Boot Keys

This force system to setup Mode-Clear all Secure Boot Variables. Change takes effect after reboot.

Enroll Efi Image

Allow the image to run in Secure Boot mode. Enroll SHA256 hash of the binary into Authorized Signature Database (db).

Export Secure Boot Variables

Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device.

Platform Key (PK)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

- a) EFI_SIGNATURE_LIST
- b) EFI_CERT_X509 (DER)
- c) EFI_CERT_RSA2048 (bin)
- d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

Key Exchange Keys (KEK)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

- a) EFI_SIGNATURE_LIST
- b) EFI_CERT_X509 (DER)
- c) EFI_CERT_RSA2048 (bin)
- d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

Authorized Signatures (db)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

- a) EFI_SIGNATURE_LIST
- b) EFI_CERT_X509 (DER)
- c) EFI_CERT_RSA2048 (bin)
- d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

Forbidden Signatures (dbx)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

- a) EFI_SIGNATURE_LIST
- b) EFI_CERT_X509 (DER)
- c) EFI_CERT_RSA2048 (bin)
- d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

Authorized TimeStamps (dbt)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

- a) EFI_SIGNATURE_LIST
- b) EFI_CERT_X509 (DER)
- c) EFI_CERT_RSA2048 (bin)
- d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

OsRecovery Signatures (dbr)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

- a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, Modified, Mixed

3.7 Boot Screen

In this section, it will display the available devices on the system for user to configure the boot settings and the boot priority.



Boot Option #1/#2/#3/#4/#5/#6

Use this to set the system boot order.

UEFI USB Drive BBS Priorities

Specifies the Boot Device Priority sequence from available UEFI USB Drives.

UEFI Application Boot Priorities

Specifies the Boot Device Priority sequence from available UEFI Application.

Setup Prompt Timeout

Configure the number of seconds to wait for the UEFI setup utility.

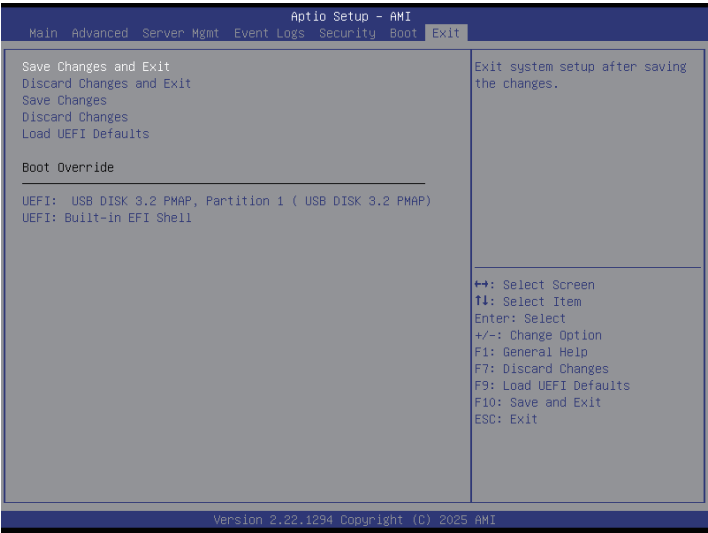
Bootup NumLock State

Select whether Num Lock should be turned on or off when the system boots up.

Full Screen Logo

Enable to display the boot logo or disable to show normal POST message.

3.8 Exit Screen



Save Changes and Exit

When selecting this option, the following message “Save configuration changes and exit setup?” will pop-out. Press <F10> key or select [Yes] to save the changes and exit the UEFI SETUP UTILITY.

Discard Changes and Exit

When selecting this option, the following message “Discard changes and exit setup?” will pop-out. Press <ESC> key or select [Yes] to exit the UEFI SETUP UTILITY without saving any changes.

Save Changes

When selecting this option, the following message “Save changes?” will pop-out. Select [Yes] to save all changes.

Discard Changes

When selecting this option, the following message “Discard changes?” will pop-out. Select [Yes] to discard all changes.

Load UEFI Defaults

Use this item to restore or load default values for all the setup options.

Chapter 4 Software Support

After all the hardware has been installed, it suggests to go to the official website at <http://www.ASRockRack.com> and make sure if there are any new updates of the BIOS / BMC firmware for the motherboard.

4.1 Download and Install Operating System

This motherboard supports various Microsoft® Windows® Server / Linux compliant operating systems. Please download the operating system from the OS manufacturer. Please refer to the OS documentation for more instructions.

**Please download the Intel® Rapid Storage Technology driver from the ASRock Rack's website (www.asrockrack.com) to the USB drive while installing OS in SATA RAID mode.*

4.2 Download and Install Software Drivers

This motherboard supports various Microsoft® Windows® compliant drivers. Please download the required drivers from the website at <http://www.ASRockRack.com>.

To download necessary drivers, go to the product page, click on the "Download" tab, choose the operating system that is used, and then download the using driver.

4.3 Contact Information

Contact ASRock Rack or want to know more about ASRock Rack, welcome to visit ASRock Rack's website at <http://www.ASRockRack.com>; or contact the dealer for further information.

Chapter 5 Troubleshooting

5.1 Troubleshooting Procedures

Follow the procedures below to troubleshoot the system.



Always unplug the power cord before adding, removing or changing any hardware components. Failure to do so may cause physical injuries and damages to motherboard components.

1. Disconnect the power cable and check whether the PWR LED is off.
2. Unplug all cables, connectors and remove all add-on cards from the motherboard.
Make sure that the jumpers are set to default settings.
3. Confirm that there are no short circuits between the motherboard and the chassis.
4. Install a CPU and fan on the motherboard, then connect the chassis speaker and power LED.

If there is no power...

1. Confirm that there are no short circuits between the motherboard and the chassis.
2. Make sure that the jumpers are set to default settings.
3. Check the settings of the 115V/230V switch on the power supply.
4. Verify if the battery on the motherboard provides ~3VDC. Install a new battery if it does not.

If there is no video...

1. Try replugging the monitor cables and power cord.
2. Check for memory errors.

If there are memory errors...

1. Verify that the DIMM modules are properly seated in the slots.
2. Use recommended DDR5 RDIMM/MRDIMM.
3. Install more than one DIMM modules that should be identical with the same brand, speed, size and chip-type.
4. Try inserting different DIMM modules into different slots to identify faulty ones.
5. Check the settings of the 115V/230V switch on the power supply.

Unable to save system setup configurations...

1. Verify if the battery on the motherboard provides ~3VDC. Install a new battery if it does not.
2. Confirm whether the power supply provides adequate and stable power.

Other problems...

1. Try searching keywords related to the related problem on ASRock Rack's FAQ page:
<http://www.asrockrack.com/support>

5.2 Technical Support Procedures

If the problems are still unsolved, please contact ASRock Rack's technical support with the following information:

1. Contact information
2. Model name, BIOS version and problem type.
3. System configuration.
4. Problem description.

Contact ASRock Rack's technical support at:
<http://www.asrockrack.com/support/tsd.asp>

5.3 Returning Merchandise for Service

For warranty service, the receipt or a copy of the invoice marked with the date of purchase is required. By calling the vendor or going to RMA website (<http://event.asrockrack.com/tsd.asp>) to obtain a Returned Merchandise Authorization (RMA) number.

The RMA number should be displayed on the outside of the shipping carton which is mailed prepaid or hand-carried when returning the motherboard to the manufacturer. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty does not cover damages incurred in shipping or from failure due to alteration, misuse, abuse or improper maintenance of products.

Contact the distributor first for any product related problems during the warranty period.

Contact Information

If it needs to contact ASRock Rack or want to know more about ASRock Rack, you're welcome to visit ASRock Rack's website at <http://www.asrockrack.com>; or contact the dealer for further information. For technical questions, please submit a support request form at <https://event.asrockrack.com/tsd.asp>

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