Jumpers and Headers Setting Guide

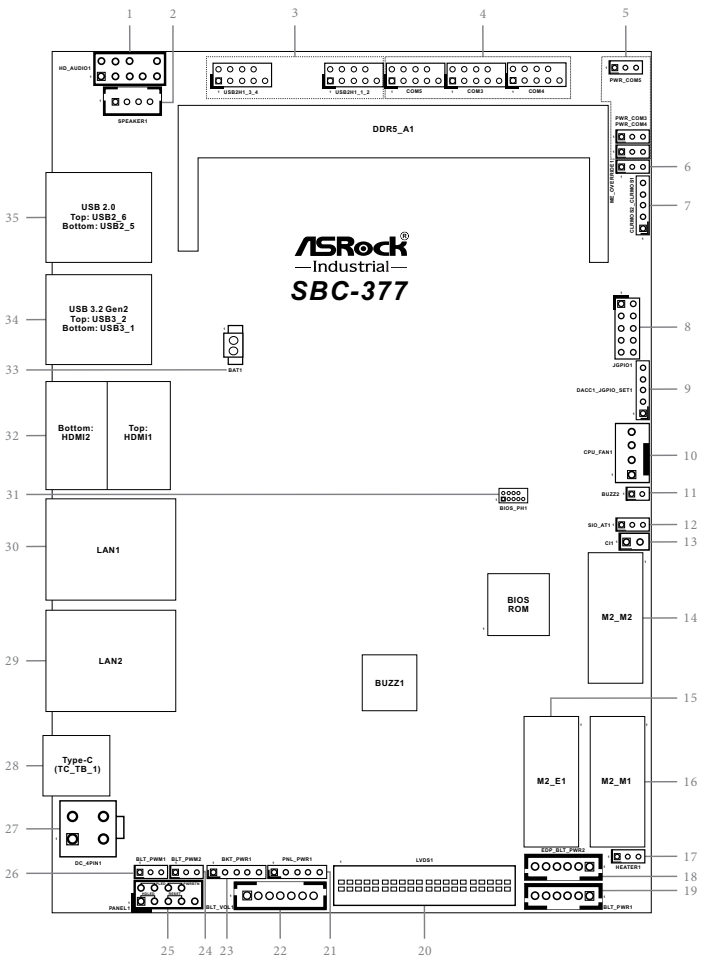
ASRock Industrial

SBC-377

Revision History

Date	Description
September 19, 2025	First Release
December 26, 2025	Second Release
February 13, 2026	Third Release

Top:



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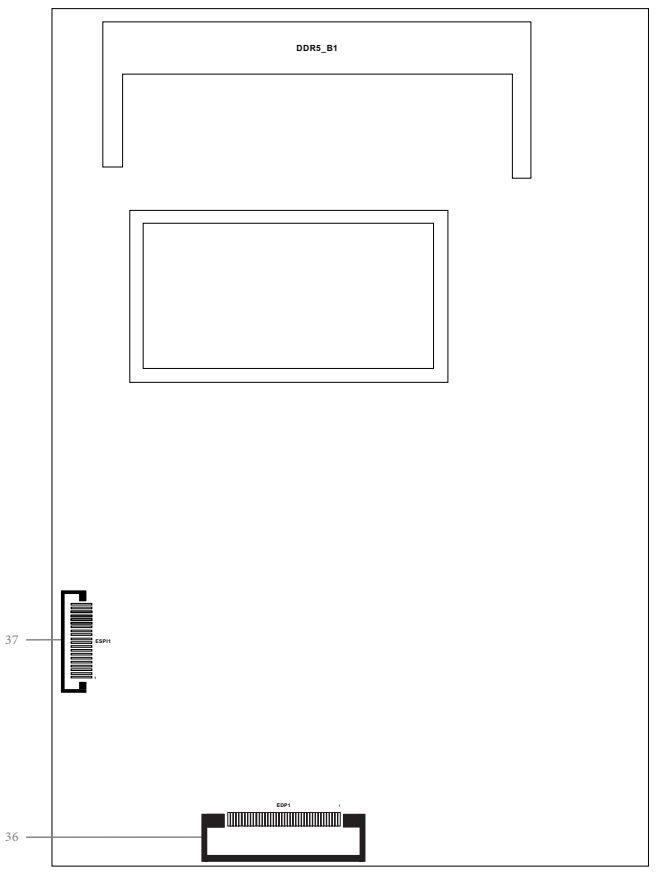
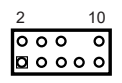


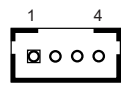
1 : Front Panel Audio Header (HD_AUDIO1)

Pin	Signal Name	Signal Name	Pin
1	MIC1_L	AGND_A	2
3	MIC1_R	NA	4
5	LINE2_R_OUT	LINE1_JD	6
7	AGND_A		8
9	LINE2_L_OUT	LINE2_JD	10



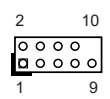
2 : 3W Audio AMP Output Wafer (SPEAKER1)

Pin	Signal Name
1	OUTLN
2	OUTLP
3	OUTRP
4	OUTRN



3 : USB 2.0 Headers (USB2H_3_4, USB2H_1_2)

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	USB_PWR	2
3	USB_D-	USB_D-	4
5	USB_D+	USB_D+	6
7	GND	GND	8
9	DUMMY		10

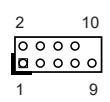


4 : COM Port Headers (COM3~5) (RS232/422/485) *

* This motherboard supports RS232/422/485 on COM3, 4 and 5 ports. Please refer to the table below for the pin definition. In addition, COM3, 4 and 5 ports (RS232/422/485) can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

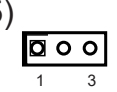
COM3, 4 and 5 Ports Pin Definition

Pin	RS232	RS422	RS485
1	DCD	TX-	RTX-
2	RXD	TX+	RTX+
3	TXD	RX+	NA
4	DTR	RX-	NA
5	GND	GND	GND
6	DSR	NA	NA
7	RTS	NA	NA
8	CTS	NA	NA
9	PWR	PWR	PWR



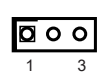
5 : COM Port Pin9 PWR Setting Jumpers

PWR_COM3 (For COM Port3)
PWR_COM4 (For COM Port4)
PWR_COM5 (For COM Port5)
Open : +0V
1-2 : +5V (Default)
2-3 : +12V



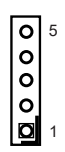
6 : ME_OVERRIDE1

1-2 : Disable ME override# (Default)
2-3 : Enable ME override#



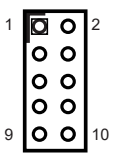
7 : Clear CMOS Header (CLRMOS2_CLRMOS1)

Pin	Signal Name
1-2	Open : Normal (Default) Short : Auto Clear CMOS (Power Off)
3-4	Normal (Default)
4-5	Clear CMOS



8 : Digital Input/Output Pin Header (JGPIO1)

Pin	Signal Name	Signal Name	Pin
1	GPP_S02_ GPO_1_3V	GPP_C22_ GPI_1_3V	2
3	GPP_S03_ GPO_2_3V	GPP_C23_ GPI_2_3V	4
5	GPP_S04_ GPO_3_3V	GPP_E00_ GPI_3_3V	6
7	GPP_S05_ GPO_4_3V	GPP_D03_ GPI_4_3V	8
9	DIO_PWR_+5V	GND	10



Parameter	Range
GPIO Input Low Voltage	Max: 1.15V
GPIO Input High Voltage	Min: 2.15V
GPIO Output Low Voltage	Max: 0.45V
GPIO Output High Voltage	Min: 2.85V
Note: Max. load per GPI/O pin: 2mA Current Max. 1A per pin	

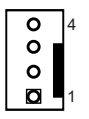
9 : DACC & Digital Input/Output Default Value Setting (DACC1_JGPIO_SET1)

1-2 Open : no ACC
1-2 Short : ACC (Default)*
3-4 : +3V (Default)
4-5 : GND

* Auto clear CMOS when system boot improperly.

10 : CPU FAN Connector (+12V) (CPU_FAN1)

Pin	Signal Name
1	GND
2	+12V
3	CPU_FAN_SPEED
4	FAN_SPEED_CONTROL



11 : Buzzer Header (BUZZ2)

Pin	Signal Name
1	BUZZ_LOW
2	+5V

12 : ATX/AT Mode Jumper (SIO_AT1)

1-2 : ATX Mode (Default)
2-3 : AT Mode

13 : Chassis Intrusion Header (CI1)

Open : Normal (Default)
Short : Active Case Open

17 : Heater header (HEATER1)

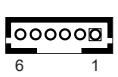
Pin	Signal Name
1	Heater_PWR (5V/1A)
2	GND
3	NTC (Negative Temperature Coefficient) thermistors

• The 10k Ohm NTC thermistors is suggested.

• Deep mode is not supported when the preheat function is enabled.

18 : eDP Inverter Power Control Wafer (EDP_BLT_PWR2)

Pin	Signal Name
1	GND
2	GND
3	EDP_LBKLT_CTL
4	EDP_LBKLT_EN
5	+12V
6	+12V



M.2 Key-M Sockets

14 : M2_M2

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	PERn3	NA	6
7	PERp3	NA	8
9	GND	SATA_LED	10
11	PETn3	+3.3V	12
13	PETp3	+3.3V	14
15	GND	+3.3V	16
17	PERn2	+3.3V	18
19	PERp2	NA	20
21	GND	NA	22
23	PETn2	NA	24
25	PETp2	NA	26
27	GND	NA	28
29	PERn1	NA	30
31	PERp1	GND	32
33	GND	USB_D+	34
35	PETn1	USB_D-	36
37	PETp1	GND	38
39	GND	SMB_CLK	40
41	PERn0	SMB_DATA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETP0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

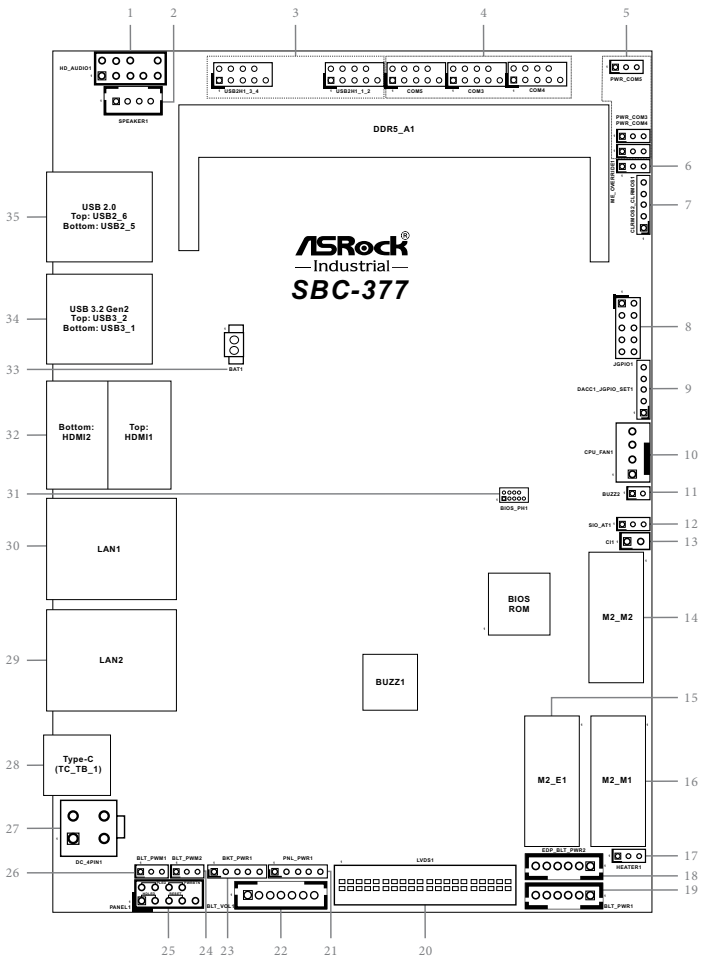
16 : M2_M1

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	PERn3	NA	6
7	PERp3	NA	8
9	GND	SATA_LED	10
11	PETn3	+3.3V	12
13	PETp3	+3.3V	14
15	GND	+3.3V	16
17	PERn2	+3.3V	18
19	PERp2	NA	20
21	GND	NA	22
23	PETn2	NA	24
25	PETp2	NA	26
27	GND	NA	28
29	PERn1	NA	30
31	PERp1	NA	32
33	GND	NA	34
35	PETn1	NA	36
37	PETp1	NA	38
39	GND	SMB_CLK	40
41	PERn0	SMB_DATA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETP0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

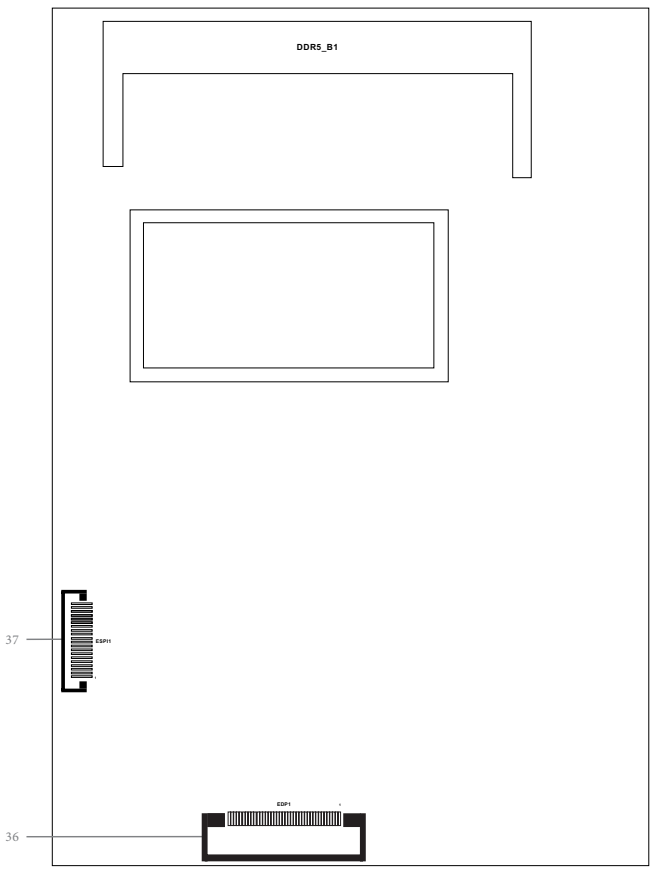
15 : M.2 Key-E Socket (M2_E1)

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	USB_D+	+3.3V	4
5	USB_D-	NA	6
7	GND	NA	8
9	CNV_WGR_D1-	CNV_RF_RESET	10
11	CNV_WGR_D1+	NA	12
13	GND	MODEM_CLKREQ	14
15	CNV_WGR_D0-	NA	16
17	CNV_WGR_D0+	GND	18
19	GND	NA	20
21	CNV_WGR_CLK-	CNV_BRI_RSP	22
23	CNV_WGR_CLK+		
		CNV_BGI_DT	32
33	GND	CNV_RGI_RSP	34
35	PETp	CNV_BRI_DT	36
37	PETn	NA	38
39	GND	NA	40
41	PERp	NA	42
43	PERn	NA	44
45	GND	NA	46
47	PEFCLKp	NA	48
49	PEFCLKn	SUSCLK	50
51	GND	PERST0#	52
53	CLKREQ#	W_DISABLE1#	54
55	NA	W_DISABLE2#	56
57	GND	SMB_DATA	58
59	CNV_WT_D1-	SMB_CLK	60
61	CNV_WT_D1+	NA	62
63	GND	NA	64
65	CNV_WT_D0-	NA	66
67	CNV_WT_D0+	NA	68
69	GND	NA	70
71	CNV_WT_CLK-	+3.3V	72
73	CNV_WT_CLK+	+3.3V	74
75	GND		

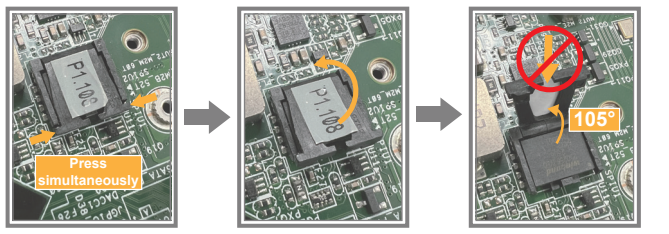
Top:

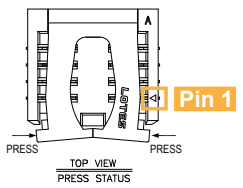


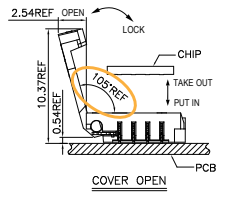
Bottom:



Installation of LOTES ROM Socket







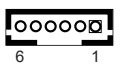
- Do not press one side of the actuator cover at a time. Always apply even and simultaneous force to both sides to avoid damage.
- Do not apply force to the actuator cover after the IC is inserted, especially when it is fully opened at 105 degrees. Pressing vertically at this angle may cause the cover to break.

- The white dot (Pin 1) on the ROM must align with the Pin 1 position of the socket (white arrow area).
- Ensure the white dot on the ROM is facing outward from the socket.

Warning: Incorrect installation may damage the chipset and motherboard. Refer to the picture for proper orientation.

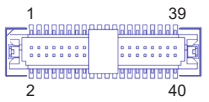
19 : Inverter Power Control Wafer (BLT_PWR1)

Pin	Signal Name
1	GND
2	GND
3	CON_LBKLT_CTL
4	CON_LBKLT_EN
5	+LCD_BLT_VCC
6	+LCD_BLT_VCC



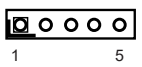
20 : LVDS Panel Connector (LVDS1)*

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	+3.3V	NA	4
5	NA	LVDS_A_DATA0#	6
7	LVDS_A_DATA0	GND	8
9	LVDS_A_DATA1#	LVDS_A_DATA1	10
11	GND	LVDS_A_DATA2#	12
13	LVDS_A_DATA2	GND	14
15	LVDS_A_DATA3#	LVDS_A_DATA3	16
17	GND	LVDS_A_CLK#	18
19	LVDS_A_CLK	GND	20
21	LVDS_B_DATA0#	LVDS_B_DATA0	22
23	GND	LVDS_B_DATA1#	24
25	LVDS_B_DATA1	GND	26
27	LVDS_B_DATA2#	LVDS_B_DATA2	28
29	DPLVDD_EN	LVDS_B_DATA3#	30
31	LVDS_B_DATA3	GND	32
33	LVDS_B_CLK#	LVDS_B_CLK	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40



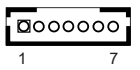
21 : Panel Power Select (LCD_VCC) (PNL_PWR1)

1-2: LCD_VCC : +3V (Default)
2-3: LCD_VCC : +5V
4-5: LCD_VCC : +12V



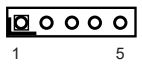
22 : Backlight Volume Control (BLT_VOL1)

Pin	Signal Name
1	GPIO_VOL_UP
2	GPIO_VOL_DN
3	PWRDN
4	BLT_UP
5	BLT_DN
6	GND
7	GND



23 : Backlight Power Select (LCD_BLT_VCC) (BKT_PWR1)

1-2: LCD_BLT_VCC: +5V (Default)
2-3: LCD_BLT_VCC: +12V
4-5: LCD_BLT_VCC: DC_IN

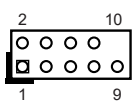


24 : CON_LBKLT_CTL Voltage Level (BLT_PWM2)

1-2 : 3V Level (Default)
2-3 : 5V Level

25 : System Panel Header (PANEL1)

Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	+5VSB		10



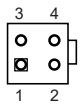
26 : Brightness Control Mode (BLT_PWM1)

1-2 : From eDP PWM to CON_LBKLT_CTL
2-3 : From LVDS PWM to CON_LBKLT_CTL (Default)

- Please set to 1-2 when adjusting brightness by Brightness Control bar under OS.
- Please set to 2-3 when adjusting brightness by BLT_VOL1.

27 : 4-pin ATX PWR Connector (DC_4PIN1)

Pin	Signal Name	Signal Name	Pin
1	GND	GND	2
3	DC Input	DC Input	4



28 : Type-C Port (TC_TB_1)

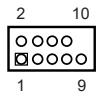
* supports sink mode: 20V/5A 100W DC-IN or source mode: 5V/3A USB3+DP

29 : RJ45 LAN Port (LAN2)

30 : RJ45 LAN Port (LAN1)

31 : BIOS_PH1

Pin	Signal Name	Signal Name	Pin
1	F1_SPI_CS#	+1.8VSB_SPI_FLASH	2
3	F1_SPI_MISO	F1_SPI_DQ3	4
5	F1_SPI_DQ2	F1_SPI_CLK	6
7	RSMRST#	F1_SPI_MOSI	8
9	GND		10



32 : USB 3.2 Gen2 Ports

Top : USB3_2
Bottom : USB3_1

33 : Battery Connector (BAT1)

Pin	Signal Name
1	+BAT
2	GND

34 : USB 3.2 Gen2 Ports

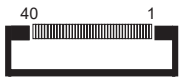
Top : USB3_2
Bottom : USB3_1

35 : USB 2.0 Ports

Top : USB2_6
Bottom : USB2_5

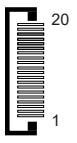
Back Side :

36 : eDP Connector (EDP1)



Pin	Signal Name
1	NA
2	GND
3	eDP_TX#3_CON
4	eDP_TX3_CON
5	GND
6	eDP_TX#2_CON
7	eDP_TX2_CON
8	GND
9	eDP_TX#1_CON
10	eDP_TX1_CON
11	GND
12	eDP_TX#0_CON
13	eDP_TX0_CON
14	GND
15	eDP_AUX_CON
16	eDP_AUX#_CON
17	GND
18	LCD_VCC
19	LCD_VCC
20	LCD_VCC
21	LCD_VCC
22	NA
23	GND
24	GND
25	GND
26	GND
27	eDP_HPD_CON
28	GND
29	GND
30	GND
31	GND
32	eDP_BKLTEN
33	eDP_BKLTCTL_R
34	SMB_DATA_MAIN
35	SMB_CLK_MAIN
36	+12V
37	+12V
38	+12V
39	+12V
40	NA

37 : ESPI Header (ESPI1)



Pin	Signal Name
1	GND
2	ESPI_CLK
3	GND
4	ESPI_CS0_N
5	ESPI_RESET_N
6	GND
7	+3V
8	
9	
10	
11	ESPI_IO0
12	ESPI_IO1
13	ESPI_IO2
14	ESPI_IO3
15	
16	+3VSB
17	G3_AT_GPIO#
18	
19	ESPI_ALERT0_N
20	GND