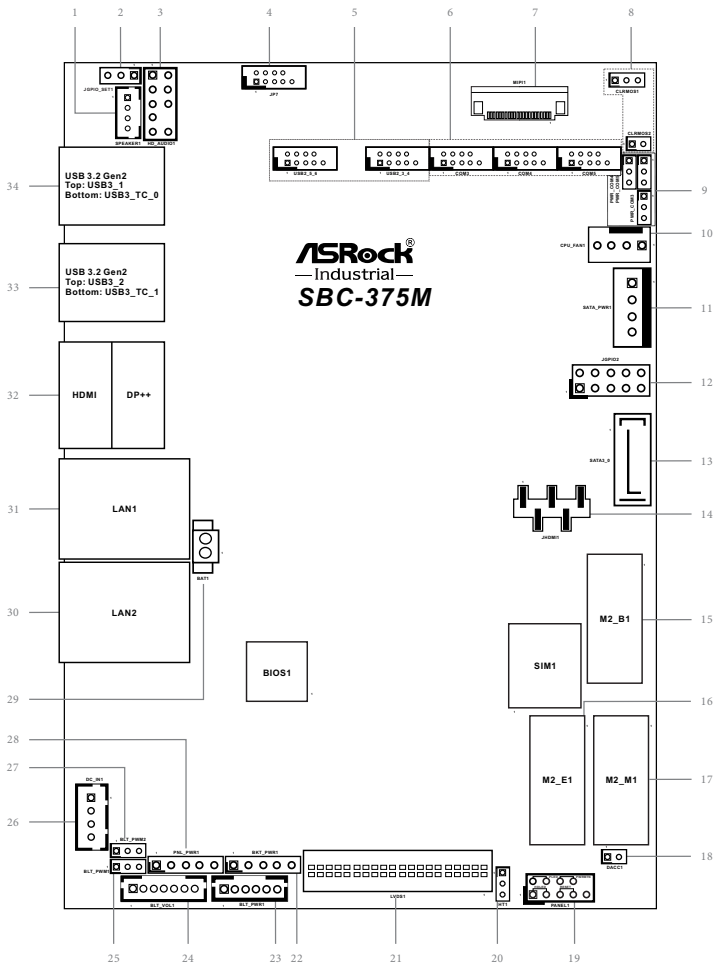
Jumpers and Headers Setting Guide

SBC-375P
SBC-375M

Revision History

Date	Description
March 7, 2024	First Release
May 29, 2024	Second Release
July 16, 2024	Third Release
September 2, 2024	Fourth Release
January 21, 2025	Fifth Release
May 9, 2025	Sixth Release
June 16, 2025	Seventh Release
October 23, 2025	Eighth Release

Top:



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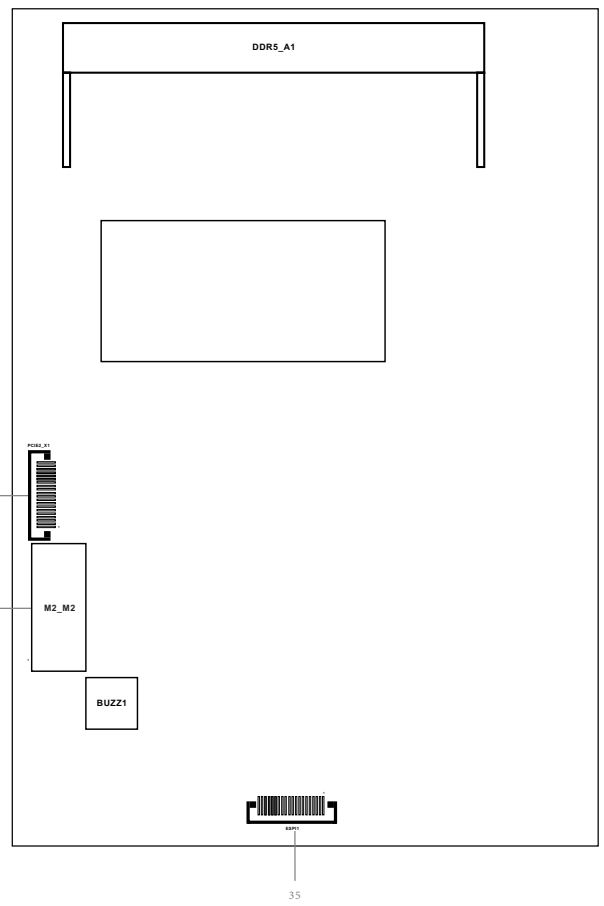
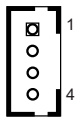


1 : 3W Audio AMP Output Wafer (SPEAKER1)

Pin	Signal Name
1	OUTLN
2	OUTLP
3	OUTRP
4	OUTRN

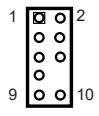


2 : Digital Input/Output Default Value Setting (JGPIO_SET1)

1-2 : +3V (Default)
2-3 : GND

3 : Front Panel Audio Header (HD_AUDIO1)

Pin	Signal Name	Signal Name	Pin
1	MIC1_L	AGND_A	2
3	MIC1_R	NA	4
5	LINE2_R_OUT	LINE1_JD	6
7	AGND_A		8
9	LINE2_L_OUT	LINE2_JD	10



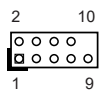
4 : JP7

<Test CI1 (Normally open)>
JP7: 24 (Connect to Case)

<AT_ATX_Mode>
JP7: 13 (Open) = ATX Mode (Default)
JP7: 13 (Short) = AT Mode

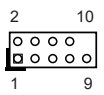
<Buzzer Header>
JP5: Buzzer
JP7: +5V

Pin	Signal Name	Signal Name	Pin
1	AT_ATX_Mode	CASEOPEN#_CI1	2
3	GND	GND	4
5	Buzzer	GND	6
7	+5V	NA	8
9	NA		10



5 : USB 2.0 Headers (USB2_5_6, USB2_3_4)

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	USB_PWR	2
3	USB_D-	USB_D-	4
5	USB_D+	USB_D+	6
7	GND	GND	8
9	DUMMY		10

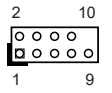


6 : COM Port Headers (COM3~5) (RS232/422/485) *

* This motherboard supports RS232/422/485 on COM3, 4 and 5 ports. Please refer to the table below for the pin definition. In addition, COM3, 4 and 5 ports (RS232/422/485) can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

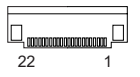
COM3, 4 and 5 Ports Pin Definition

Pin	RS232	RS422	RS485
1	DCD	TX-	RTX-
2	RXD	TX+	RTX+
3	TXD	RX+	N/A
4	DTR	RX-	N/A
5	GND	GND	GND
6	DSR	N/A	N/A
7	RTS	N/A	N/A
8	CTS	N/A	N/A
9	PWR	PWR	PWR



7 : MIPI Connector (MIPI1)

Pin	Signal Name
1	+3V
2	I2C0_SDA_CAM_3V
3	I2C0_SCL_CAM_3V
4	GND
5	CAM_MCLK_3V
6	CAM_RST_PWDN_3V
7	GND
8	CSI_E_D3_DP
9	CSI_E_D3_DN
10	GND
11	CSI_E_D2_DP
12	CSI_E_D2_DN
13	GND
14	CSI_E_CK_DP
15	CSI_E_CK_DN
16	GND
17	CSI_E_D1_DP
18	CSI_E_D1_DN
19	GND
20	CSI_E_D0_DP
21	CSI_E_D0_DN
22	GND



8 : Clear CMOS Headers CLRMOS1

1-2 : Normal (Default)
2-3 : Clear CMOS

CLRMOS2

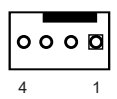
Open : Normal (Default)
Short : Auto Clear CMOS (Power Off)

9 : COM Port Pin9 PWR Setting Jumpers

PWR_COM3 (For COM Port3)
PWR_COM4 (For COM Port4)
PWR_COM5 (For COM Port5)
1-2 : +5V (Default)
2-3 : +12V
Open: +0V

10 : CPU FAN Connector (+12V) (CPU_FAN1)

Pin	Signal Name
1	GND
2	+12V
3	CPU_FAN_SPEED
4	FAN_SPEED_CONTROL

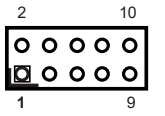


11 : SATA Power Output Connector (SATA_PWR1)

Pin	Signal Name
1	+5V
2	GND
3	GND
4	+12V

12 : Digital Input/Output Pin Header (JGPIO2)

Pin	Signal Name	Signal Name	Pin
1	GPP_S02	GPP_C22	2
3	GPP_S03	GPP_C23	4
5	GPP_S04	GPP_E00	6
7	GPP_S05	GPP_D03	8
9	DIO_PWR_+5V	GND	10



Pin	Signal Name
GPIO Input Low Voltage	Max: 0.15V
GPIO Input High Voltage	Min: 2.9V
GPIO Output Low Voltage	Max: 0.55V
GPIO Output High Voltage	Min: 2.2V

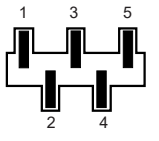
Note:
Max. load per GPI/O pin: 0.85mA
Current Max. 1A per pin

13 : SATA3 Connector (SATA3_0)

Pin	Signal Name
1	GND
2	SATA_0_TX_DP_C
3	SATA_0_TX_DN_C
4	GND
5	SATA_0_RX_DN_C
6	SATA_0_RX_DP_C
7	GND

14 : JHDMI1(For HDMI-MIPI Card)

Pin	Signal Name
1	+5V
2	GND
3	GPP_V23
4	GPP_V22
5	GPP_C8



15 : M.2 Key-B Socket (M2_B1)

Pin	Signal Name	Signal Name	Pin
1	NA	+3.3V	2
3	GND	+3.3V	4
5	GND	FuLL_Card_Power_off	6
7	USB_D+	W_DISABLE	8
9	USB_D-	WWAN_LED#	10
11	GND		
		NA	20
21	GND	NA	22
23	NA	NA	24
25	NA	NA	26
27	GND	NA	28
29	USB3_RX-	UIM_RESET	30
31	USB3_RX+	UIM_CLK	32
33	GND	UIM_DATA	34
35	USB3_TX-	UIM_PWR	36
37	USB3_TX+	NA	38
39	GND	SMB_CLK	40
41	PERn0	SMB_DATA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETP0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
59	NA	NA	60
61	NA	NA	62
63	NA	NA	64
65	NA	NA	66
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	NA		

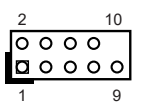
18 : DACC1

Open: no ACC
Short: ACC (Default)

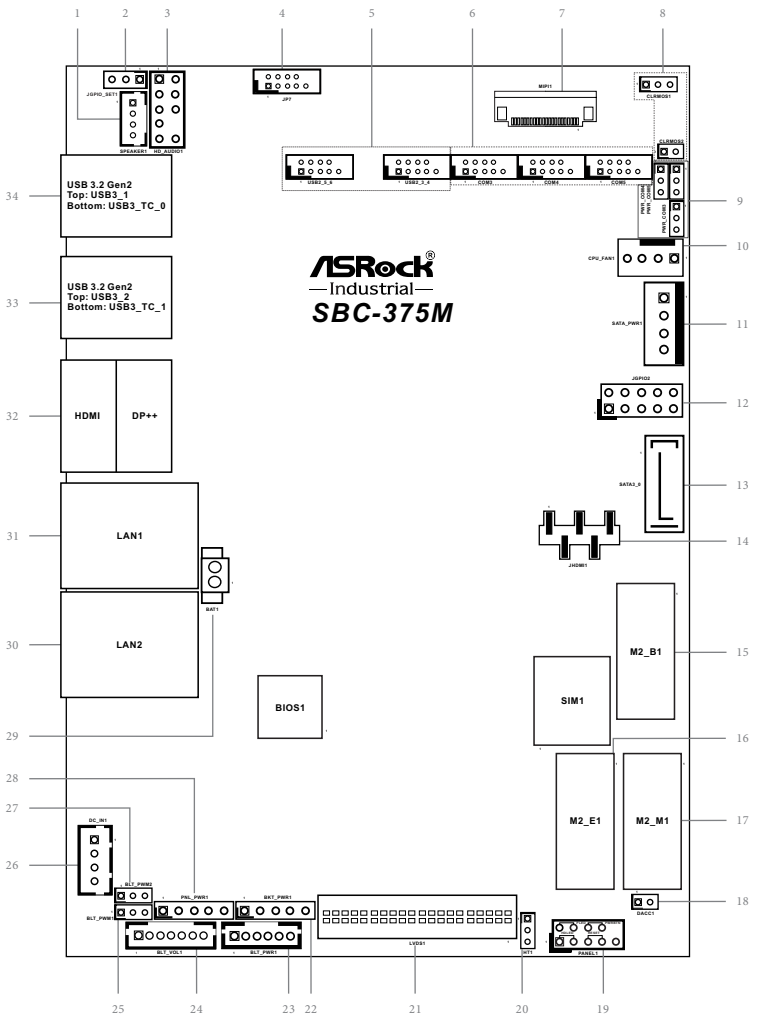
• Auto clear CMOS when system boot improperly.

19 : System Panel Header (PANEL1)

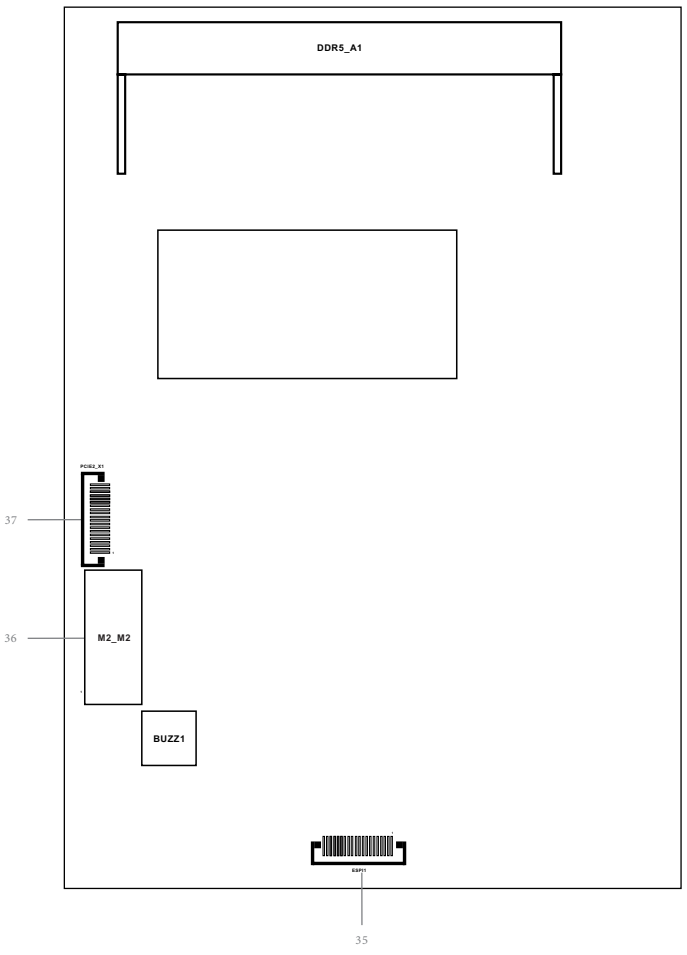
Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	+5VSB		10



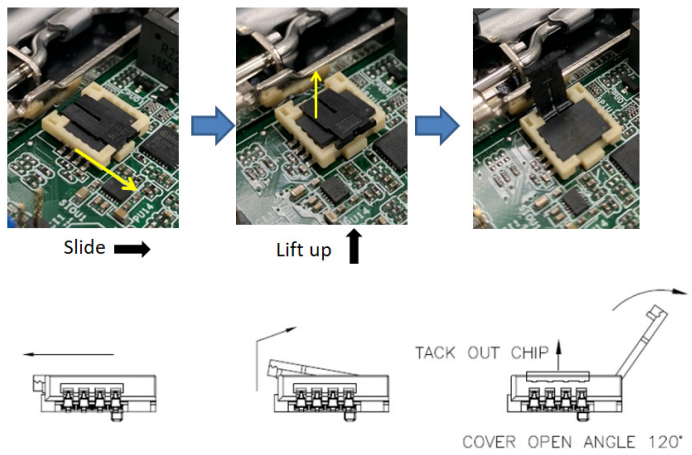
Top:



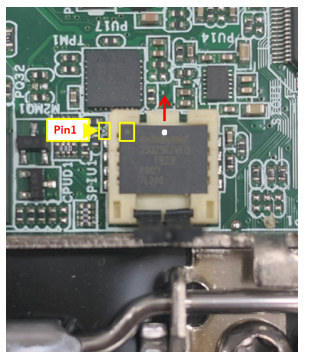
Bottom:



Installation of ROM Socket



* Do not apply force to the actuator cover after ic inserted.
* Do not apply force to actuator cover when it is opening over 120 degree, Otherwise, the actuator cover may be broken.



* The yellow dot (Pin1) on the ROM must be installed at pin1 position of the socket (white arrow area).
* Make sure the white dot on the ROM is installed outwards of the socket.
* For further details of how to install ROM, please refer to ASRI website.

Warning: If the installation does not follow as the picture, then it may cause severe damage to chipset & MB.

16 : M.2 Key-E Socket (M2_E1)

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	USB_D+	+3.3V	4
5	USB_D-	NA	6
7	GND	NA	8
9	CNV_WGR_D1-	CNV_RF_RESET	10
11	CNV_WGR_D1+	NA	12
13	GND	MODEM_CLKREQ	14
15	CNV_WGR_D0-	NA	16
17	CNV_WGR_D0+	GND	18
19	GND	NA	20
21	CNV_WGR_CLK-	CNV_BRI_RSP	22
23	CNV_WGR_CLK+		
		CNV_BGI_DT	32
33	GND	CNV_RGI_RSP	34
35	PETp	CNV_BRI_DT	36
37	PETn	NA	38
39	GND	NA	40
41	PERp	NA	42
43	PERn	NA	44
45	GND	NA	46
47	PEFCLKp	NA	48
49	PEFCLKn	NA	50
51	GND	PERST0#	52
53	CLKREQ#	W_DISABLE1#	54
55	NA	W_DISABLE2#	56
57	GND	SMB_DATA	58
59	CNV_WT_D1-	SMB_CLK	60
61	CNV_WT_D1+	NA	62
63	GND	NA	64
65	CNV_WT_D0-	NA	66
67	CNV_WT_D0+	NA	68
69	GND	NA	70
71	CNV_WT_CLK-	+3.3V	72
73	CNV_WT_CLK+	+3.3V	74
75	GND		

M.2 Key-M Sockets

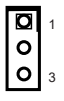
17 : M2_M1

36 : M2_M2 (on the back side)

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	PERn3	NA	6
7	PERp3	NA	8
9	GND	SATA_LED	10
11	PETn3	+3.3V	12
13	PETp3	+3.3V	14
15	GND	+3.3V	16
17	PERn2	+3.3V	18
19	PERp2	NA	20
21	GND	NA	22
23	PETn2	NA	24
25	PETp2	NA	26
27	GND	NA	28
29	PERn1	NA	30
31	PERp1	NA	32
33	GND	NA	34
35	PETn1	NA	36
37	PETp1	NA	38
39	GND	M2_M1: SMB_CLK M2_M2: NA	40
41	PERn0	M2_M1: SMB_DATA M2_M2: NA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETP0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

20 : Heater header (HT1)

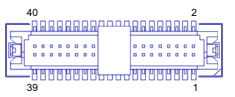
Pin	Signal Name
1	Heater_PWR (5V/1A)
2	GND
3	NTC (Negative Temperature Coefficient) thermistors



• The 10k Ohm NTC thermistors is suggested.
• Deep mode is not supported when the preheat function is enabled.

21* : LVDS Panel Connector (LVDS1)

Pin	Signal Name	Signal Name	Pin
1	+LVDD	+LVDD	2
3	+3V	eDP_LED_DRIVER	4
5	NA	LVD_A_DATA0#	6
7	LVD_A_DATA0	GND	8
9	LVD_A_DATA1#	LVD_A_DATA1	10
11	GND	LVD_A_DATA2#	12
13	LVD_A_DATA2	GND	14
15	LVD_A_DATA3#	LVD_A_DATA3	16
17	GND	LVD_A_CLK#	18
19	LVD_A_CLK	GND	20
21	LVD_B_DATA0#	LVD_B_DATA0	22
23	GND	LVD_B_DATA1#	24
25	LVD_B_DATA1	GND	26
27	LVD_B_DATA2#	LVD_B_DATA2	28
29	LVDD_EN	LVD_B_DATA3#	30
31	LVD_B_DATA3	GND	32
33	LVD_B_CLK#	LVD_B_CLK	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	+LCD_BLT_VCC	38
39	+LCD_BLT_VCC	+LCD_BLT_VCC	40

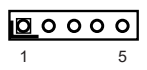


* eDP by pass mode pin definition (switch by BIOS)

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	NA	NA	4
5	NA	NA	6
7	NA	GND	8
9	EDP_TX1#	EDP_TX1	10
11	GND	EDP_TX0#	12
13	EDP_TX0	GND	14
15	NA	NA	16
17	GND	EDP_AUXN	18
19	EDP_AUXP	GND	20
21	NA	NA	22
23	GND	NA	24
25	NA	GND	26
27	NA	NA	28
29	DPLVDD_EN	NA	30
31	NA	GND	32
33	NA	NA	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40

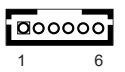
22 : Backlight Power Select (LCD_BLT_VCC) (BKT_PWR1)

1-2: LCD_BLT_VCC: +5V (Default)
2-3: LCD_BLT_VCC: +12V
4-5: LCD_BLT_VCC: DC_IN



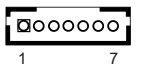
23 : Inverter Power Control Wafer (BLT_PWR1)

Pin	Signal Name
1	GND
2	GND
3	CON_LBKLT_CTL
4	CON_LBKLT_EN
5	+LCD_BLT_VCC
6	+LCD_BLT_VCC



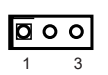
24 : Backlight Volume Control (BLT_VOL1)

Pin	Signal Name
1	GPIO_VOL_UP
2	GPIO_VOL_DN
3	PWRDN
4	BLT_UP
5	BLT_DN
6	GND
7	GND



25 : Brightness Control Mode (BLT_PWM1)

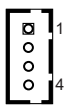
1-2 : From eDP PWM to CON_LBKLT_CTL
2-3 : From LVDS PWM to CON_LBKLT_CTL (Default)



• Please set to 1-2 when adjusting brightness by Brightness Control bar under OS.
• Please set to 2-3 when adjusting brightness by BLT_VOL1.

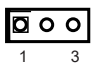
26 : 4-pin DC-in PWR Connector (Input +12V~+36V) (DC_IN1)

Pin	Signal Name
1	GND
2	DC_Input
3	DC_Input
4	GND



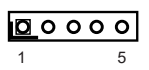
27 : CON_LBKLT_CTL Voltage Level (BLT_PWM2)

1-2 : 3V Level (Default)
2-3 : 5V Level



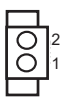
28 : Panel Power Select (LCD_VCC) (PNL_PWR1)

1-2: LCD_VCC : +3V (Default)
2-3: LCD_VCC : +5V
4-5: LCD_VCC : +12V



29 : Battery Connector (BAT1)

Pin	Signal Name
1	BAT+
2	GND



30 : RJ45 LAN Port (LAN2)

31 : RJ45 LAN Port (LAN1)

33 : Top : DisplayPort (DP++)
Bottom : HDMI Port (HDMI)

33 : Top : USB 3.2 Gen2 Port (USB3_2)
Bottom : USB 3.2 Gen2 Type-C Port (USB3_TC_1)

34 : Top : USB 3.2 Gen2 Port (USB3_1)
Bottom : USB 3.2 Gen2 Type-C Port (USB3_TC_0)

Back Side :

35 : ESPI Header (ESPI1)

Pin	Signal Name
1	GND
2	ESPI_CLK
3	GND
4	ESPI_CS0_N
5	ESPI_RESET_N
6	GND
7	+3V
8	ESPI_CS1_N
9	
10	
11	ESPI_IO0
12	ESPI_IO1
13	ESPI_IO2
14	ESPI_IO3
15	ESPI_ALERT1_N
16	+3VSB
17	G3_AT_GPIO#
18	+5VSB
19	ESPI_ALERT0_N
20	GND

37 : PCIE2_X1

Pin	Signal Name
1	+12V
2	+12V
3	PCIE2_X1_PERST#_3V
4	GND
5	CLK_GEN4_SRC5_DP
6	CLK_GEN4_SRC5_DN
7	GND
8	PCIE4_P4_TX_DP_C
9	PCIE4_P4_TX_DN_C
10	GND
11	PCIE4_P4_RX_DP
12	PCIE4_P4_RX_DN
13	GND
14	PCIE_X1_ SRCCLKREQ5#_3V
15	GND
16	+12V
17	+12V
18	+12V
19	+12V
20	+12V