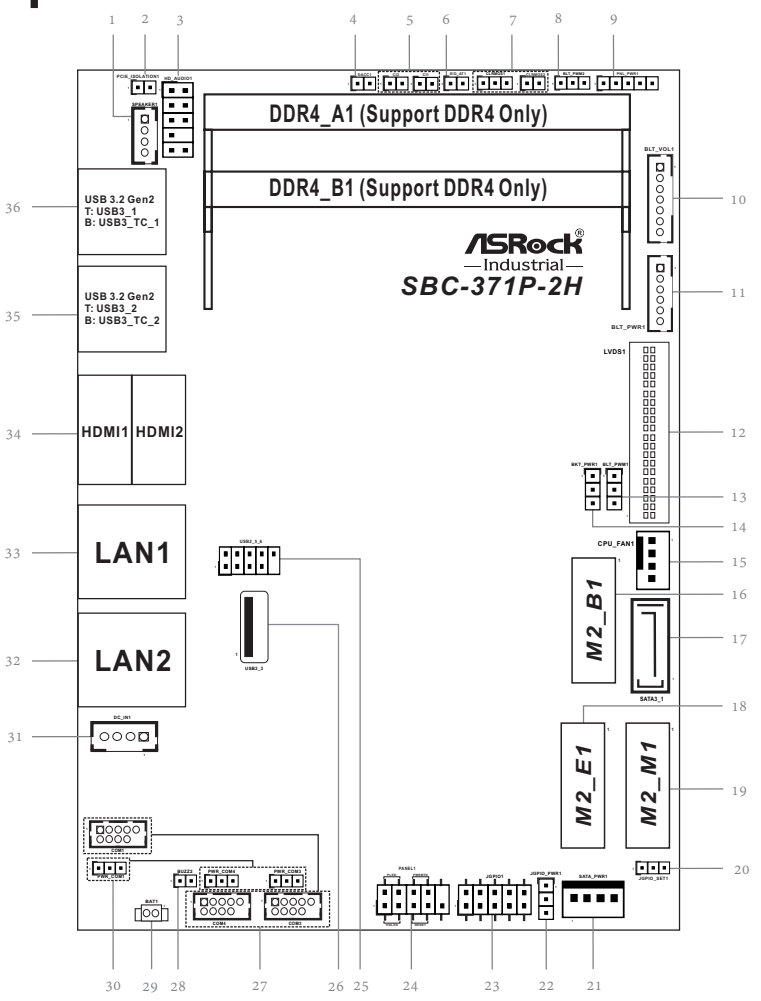
Jumpers and Headers Setting Guide

SBC-371P-2H
SBC-371M-2H
SBC-371V-2H

Revision History

Date	Description
April 21, 2025	First Release
May 15, 2025	Second Release
July 17, 2025	Third Release

Top:



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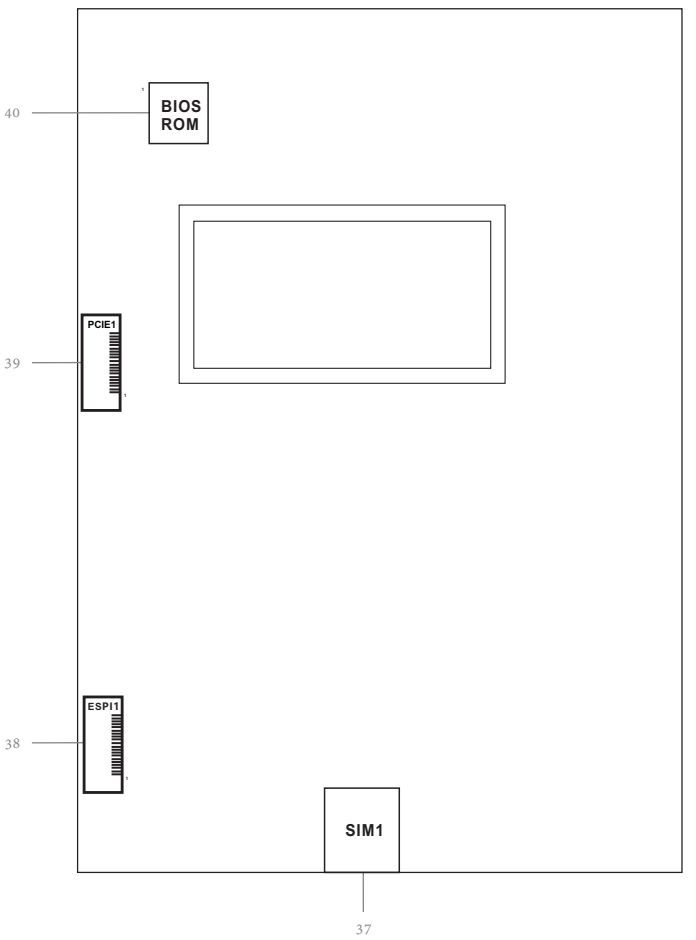
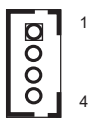


1 : 3W Audio AMP Output Wafer (SPEAKER1)

Pin	Signal Name
1	SPK L-
2	SPK L+
3	SPK R+
4	SPK R-



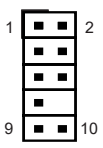
2 : PCIE_ISOLATION1

* Connect to PCIE_ISOLATION_1 header on VGA-PWR card.

Pin	Signal Name
1	PSON#
2	GND

3 : Front Panel Audio Header (HD_AUDIO1)

Pin	Signal Name	Signal Name	Pin
1	MIC1_L	AGND_A	2
3	MIC1_R	NA	4
5	LINE2_R_OUT	MIC1_JD	6
7	AGND_A		8
9	LINE2_L_OUT	LINE2_JD	10



4 : DACC Jumper (DACC1)

Open : No ACC
Short : ACC (Default)

• Auto clear CMOS when system boot improperly.

5 : Chassis Intrusion Headers (CI1, CI2)

CI1 :
Open : Normal (Default)
Short : Active Case Open

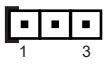
CI2 :
Open : Active Case Open
Short : Normal (Default)

6 : ATX/AT Mode Jumper (SIO_AT1)

Open : ATX Mode (Default)
Short : AT Mode

7 : Clear CMOS Headers

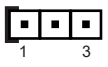
CLRMOS1 :
1-2 : Normal (Default)
2-3 : Clear CMOS



CLRMOS2 :
Open : Normal (Default)
Short : Auto Clear CMOS (Power Off)

8 : CON_LBKLT_CTL Voltage Level (BLT_PWM2)

1-2 : 3V Level (Default)
2-3 : 5V Level

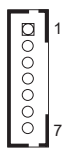


9 : Panel Power Select (LCD_VCC) (PNL_PWR1)

1-2 : +3V (Default)
2-3 : +5V
3-4 : +5V
4-5 : +12V

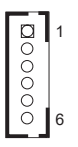
10 : Backlight & Amp Volume Control (BLT_VOL1)

Pin	Signal Name
1	NA
2	NA
3	PWRDN
4	GPIO_BLT_UP
5	GPIO_BLT_DW
6	GND
7	GND



11 : Inverter Power Control Wafer (BLT_PWR1)

Pin	Signal Name
1	GND
2	GND
3	CON_LBKLT_CTL
4	CON_LBKLT_EN
5	LCD_BLT_VCC
6	LCD_BLT_VCC

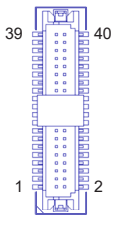


12 : LVDS Panel Connector (LVDS1)

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	+3.3V	NA	4
5	NA	LVDS_A_DATA0#	6
7	LVDS_A_DATA0	GND	8
9	LVDS_A_DATA1#	LVDS_A_DATA1	10
11	GND	LVDS_A_DATA2#	12
13	LVDS_A_DATA2	GND	14
15	LVDS_A_DATA3#	LVDS_A_DATA3	16
17	GND	LVDS_A_CLK#	18
19	LVDS_A_CLK	GND	20
21	LVDS_B_DATA0#	LVDS_B_DATA0	22
23	GND	LVDS_B_DATA1#	24
25	LVDS_B_DATA1	GND	26
27	LVDS_B_DATA2#	LVDS_B_DATA2	28
29	DPLVDD_EN	LVDS_B_DATA3#	30
31	LVDS_B_DATA3	GND	32
33	LVDS_B_CLK#	LVDS_B_CLK	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40

* eDP by pass mode pin definition (switch by BIOS)

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	NA	NA	4
5	NA	NA	6
7	NA	GND	8
9	EDP_TX1#	EDP_TX1	10
11	GND	EDP_TX0#	12
13	EDP_TX0	GND	14
15	NA	NA	16
17	GND	EDP_AUXN	18
19	EDP_AUXP	GND	20
21	NA	NA	22
23	GND	NA	24
25	NA	GND	26
27	NA	NA	28
29	DPLVDD_EN	NA	30
31	NA	GND	32
33	NA	NA	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40



13 : Brightness Control Mode (BLT_PWM1)

1-2 : From eDP PWM to CON_LBKLT_CTL
2-3 : From LVDS PWM to CON_LBKLT_CTL (Default)

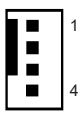
* Please set to 1-2 when adjusting brightness by Brightness Control bar under OS.
* Please set to 2-3 when adjusting brightness by BLT_VOL1.

14 : Backlight Power Select (LCD_BLT_VCC) (BKT_PWR1)

1-2 : LCD_BLT_VCC : +5V (Default)
2-3 : LCD_BLT_VCC : +12V

15 : 4-Pin CPU FAN Connector (+12V)

Pin	Signal Name
1	GND
2	+12V
3	CPU_FAN_SPEED
4	FAN_SPEED_CONTROL



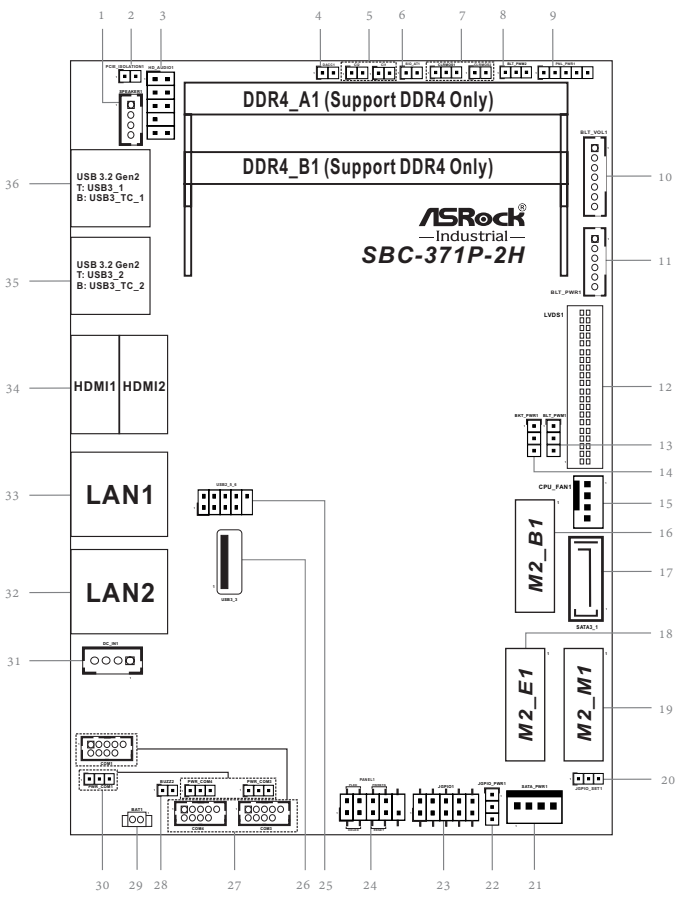
16 : M.2 Key-B Socket (M2_B1)

Pin	SIGNAL	SIGNAL	Pin
2	+3V_M2B	CONFIG_3	1
4	+3V_M2B	GND	3
6	Full_Card_Power_Off#	GND	5
8	W_DISABLE1_B#	LP+4	7
10	WWAN_LED#	LP-4	9
		GND	11
20	NC		
22	NC	NC	21
24	NC	WAKE_ON_WAN#	23
26	W_DISABLE2_B#	DPR	25
28	NC	GND	27
30	UIM1_RESET	USB3_RX4_N	29
32	UIM1_CLK	USB3_RX4_P	31
34	UIM1_DATA	GND	33
36	+UIM1_PWR	USB3_TX4_N	35
38	NA	USB3_TX4_P	37
40	NA	GND	39
42	NA	PERn0/SATA-B+	41
44	NC	PERp0/SATA-B-	43
46	NC	GND	45
48	NC	PETn0/SATA-A-	47
50	BUF_PLT_RST#	PETp0/SATA-A+	49
52	PCIECLKRQ4#	GND	51
54	NA	M2B_CLK4N	53
56	NA	M2B_CLK4P	55
58	NA	GND	57
60	NC	NC	59
62	NC	NC	61
64	NC	NC	63
66	SIM_DETECT_1	NC	65
68	SUS_CLK	BUF_PLT_RST_N	67
70	+3V_M2B	CONFIG_1	69
72	+3V_M2B	GND	71
74	+3V_M2B	GND	73
76	NC	NC	75
78	NC	NC	77
		NC	79

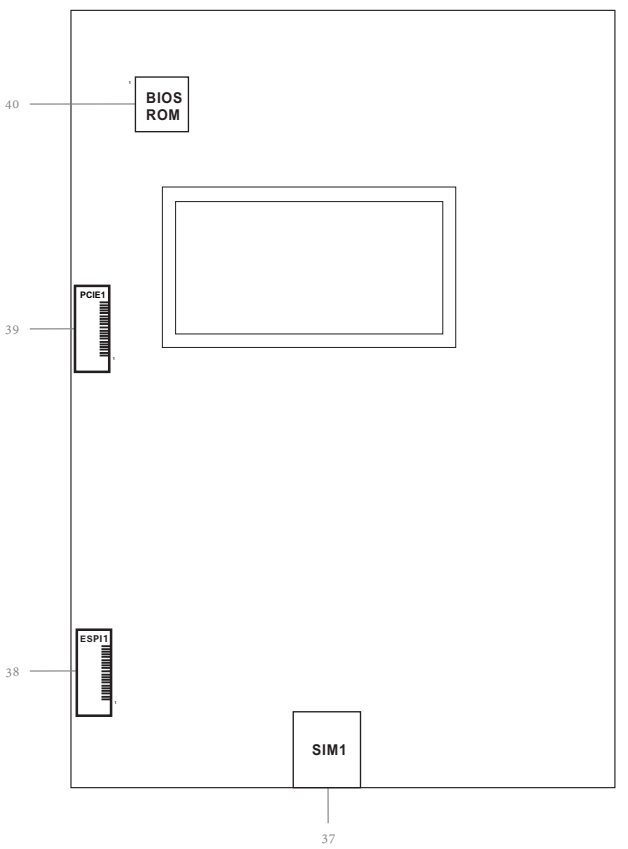
17 : SATA3 Connector (SATA3_1)

Pin	Signal Name
1	GND
2	SATA-A+
3	SATA-A-
4	GND
5	SATA-B-
6	SATA-B+
7	GND

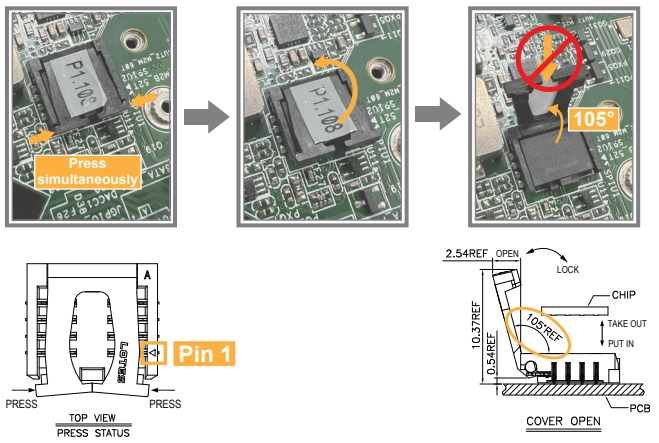
Top:



Bottom:



Installation of LOTES ROM Socket



- Do not press one side of the actuator cover at a time. Always apply even and simultaneous force to both sides to avoid damage.
- Do not apply force to the actuator cover after the IC is inserted, especially when it is fully opened at 105 degrees. Pressing vertically at this angle may cause the cover to break.

- The white dot (Pin 1) on the ROM must align with the Pin 1 position of the socket (white arrow area).
- Ensure the white dot on the ROM is facing outward from the socket.

Warning: Incorrect installation may damage the chipset and motherboard. Refer to the picture for proper orientation.

18 : M.2 Key-E Socket (M2_E1)

Pin	Signal Name	Signal Name	Pin
2	+3VSB	GND	1
4	+3VSB	LP+10	3
6	NC	LP-10	5
8	M.2_BT_PCMCLK	GND	7
10	M.2_BT_PCMFRM_CRF_RST_N	CNV_WR_D1#	9
12	M.2_BT_PCMIN	CNV_WR_D1	11
14	MODEM_CLKREQ_R	NC	13
16	NC	CNV_WR_D0#	15
18	GND	CNV_WR_D0	17
20	VRALERT#	NC	19
22	CNV_BRI_RSP	CNV_WR_CLK#	21
		CNV_WR_CLK	23
32	CNV_RGI_DT		
34	CNV_RGI_RSP	GND	33
36	CNV_BRI_DT	PCH_PE_TXP6	35
38	CL_RST#	PCH_PE_TXN6	37
40	CL_DATA	GND	39
42	CL_CLK	PCH_PE_RXP6	41
44	CNV_PA_BLANKING	PCH_PE_RXN6	43
46	CNV_MFUART2_TXD	GND	45
48	CNV_MFUART2_RXD	PCH_ECLK_WLAN1	47
50	SUS_CLK	PCH_ECLK_WLAN1#	49
52	BUF_PLT_RST_N	GND	51
54	BT_RF_KILL_N	CLKREQ1_WLAN_N	53
56	WIFI_RF_KILL_N	NA	55
58	NA	GND	57
60	NA	CNV_WT_D1#	59
62	NC	CNV_WT_D1	61
64	NC	GND	63
66	NC	CNV_WT_D0#	65
68	NC	CNV_WT_D0	67
70	NC	GND	69
72	+3VSB	CNV_WT_CLK#	71
74	+3VSB	CNV_WT_CLK	73
76	NC	GND	75
78	NC	NC	77
		NC	79

19 : M.2 Key-M Socket (M2_M1)

Pin	Signal Name	Signal Name	Pin
2	+3V	GND	1
4	+3V	GND	3
6	NC	M2M_RXN3	5
8	NC	M2M_RXP3	7
10	M2_LED	GND	9
12	+3V	M2M_TXN3	11
14	+3V	M2M_TXP3	13
16	+3V	GND	15
18	+3V	M2M_RXN2	17
20	NC	M2M_RXP2	19
22	NC	GND	21
24	NC	M2M_TXN2	23
26	NC	M2M_TXP2	25
28	NC	GND	27
30	NC	M2M_RXN1	29
32	NC	M2M_RXP1	31
34	NC	GND	33
36	NC	M2M_TXN1	35
38	NC	M2M_TXP1	37
40	NA	GND	39
42	NA	M2M_RXN0	41
44	NC	M2M_RXP0	43
46	NC	GND	45
48	NC	M2M_TXN0	47
50	BUF_PLT_RST_N	M2M_TXP0	49
52	CLKREQ0_M2M	GND	51
54	NA	M2M_CLK0N	53
56	NC	M2M_CLK0P	55
58	NC	GND	57
68	SUS_CLK	NC	67
70	+3V	+3V	69
72	+3V	GND	71
74	+3V	GND	73
76	NC	GND	75
78	NC	NC	77
		NC	79

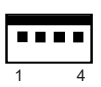
20 : GPIO Default Setting (JGPIO_SET1)

1-2 : Pull-High (Default)

2-3 : Pull-Low

21 : SATA Power Output Connector

Pin	Signal Name
1	+5V
2	GND
3	GND
4	+12V



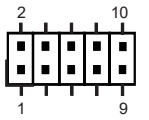
22 : Digital Input / Output Power Select (JGPIO_PWR1)

1-2 : +12V

2-3 : +5V (Default)

23 : Digital Input / Output Pin Header (JGPIO1)

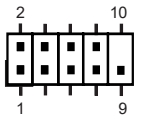
Pin	Signal Name	Signal Name	Pin
1	SIO_GP71	GPP_B15	2
3	SIO_GP72	GPP_E1	4
5	SIO_GP73	GPP_E2	6
7	SIO_GP74	GPP_E13	8
9	JGPIOPWR	GND	10



Parameter	Range
GPIO input Low voltage	Max: 0.8V
GPIO input High voltage	Low: 2V
GPIO output Low voltage	Max: 0.4V
GPIO output High voltage	Low: 2.4V
Note: Max. load per GPI/O pin: 12mA Current Max. 1A per power pin.	

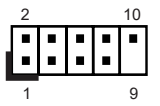
24 : System Panel Header

Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	GND		10



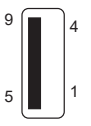
25 : USB 2.0 Connector (USB2_5_6)

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	USB_PWR	2
3	P-	P-	4
5	P+	P+	6
7	GND	GND	8
9		DUMMY	10



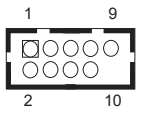
26 : USB 3.2 Gen2 Port (USB3_3)

Pin	Signal Name
1	USB_PWR
2	USB_D-
3	USB_D+
4	GND
5	SSRX-
6	SSRX+
7	GND
8	SSTX-
9	SSTX+



27 : COM1, 3, 4 Headers (COM1, 3, 4) (RS232/422/485)

Pin	Signal Name	Signal Name	Pin
1	DDCD#	RRXD	2
3	TTXD	DDTR#	4
5	GND	DDSR#	6
7	RRTS#	CCTS#	8
9	PWR		10



* This motherboard supports RS232/422/485 on COM1, 3, 4 ports. Please refer to the table below for the pin definition. In addition, COM1, 3, 4 ports (RS232/422/485) can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

COM1, 3, 4 Ports Pin Definition

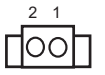
Pin	RS232	RS422	RS485
1	DCD	TX-	RTX-
2	RXD	TX+	RTX+
3	TXD	RX+	NA
4	DTR	RX-	NA
5	GND	GND	GND
6	DSR	NA	NA
7	RTS	NA	NA
8	CTS	NA	NA
9	PWR	PWR	PWR

28 : Buzzer

Pin	Signal Name
1	+5V
2	BUZZ

29 : Battery Connector

Pin	Signal Name
1	+BAT
2	GND



30 : COM Port Pin9 PWR Setting Jumpers

PWR_COM1 (For COM Port1)

PWR_COM4 (For COM Port4)

PWR_COM3 (For COM Port3)

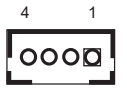
1-2 : +5V (Default)

2-3 : +12V

31 : 4-pin DC-in PWR Connector (Input 12V-36V (Default); 12V only (by BOM option))

1-4 : GND

2-3 : DC Input



* +12V PWR in --- system loading under 65W

+19V PWR in --- system loading under 95W

PWR in ≥ +24V for system loading over 95W

32 : RJ45 LAN Port (LAN2)

33 : RJ45 LAN Port (LAN1) (supports vPro)

34 : Top : HDMI Port (HDMI2)

Bottom : HDMI Port (HDMI1)

35 : Top : USB3.2 Gen2 Port (USB3_2)

Bottom : USB3.2 Gen2x2 Type-C Ports (USB3_TC_2)

36 : Top : USB3.2 Gen2 Port (USB3_1)

Bottom : USB3.2 Gen2x2 Type-C Ports (USB3_TC_1)

<u>Back Side:</u>

37 : SIM Card Socket (SIM1)

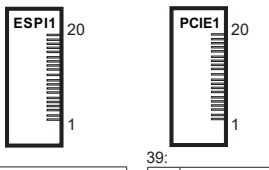
38 : ESPI Connector (ESPI1)

39 : PCIE Connector (PCIE1)*

* Supports PCIE devices up to 10W.

40 : BIOS ROM Socket

* The thermal solution of whole system needs to be designed additionally.



38:

Pin	Signal Name
20	GND
19	ESPI_ALERT#
18	Internal use
17	Internal use
16	+3VSB
15	GND
14	ESPI_IO3
13	ESPI_IO2
12	ESPI_IO1
11	ESPI_IO0
10	SMB_DATA
9	SMB_CLK
8	GND
7	+3V
6	GND
5	ESPI_RESET#
4	ESPI_CS#
3	GND
2	ESPI_CLK
1	GND

39:

Pin	Signal Name
20	+12V
19	+12V
18	+12V
17	+12V
16	+12V
15	GND
14	CLKREQ#
13	GND
12	PCIE_RXN
11	PCIE_RXP
10	GND
9	PCIE_TXN
8	PCIE_TXP
7	GND
6	CLKN
5	CLKP
4	GND
3	PLT_RST#
2	+12V
1	+12V