

Top:

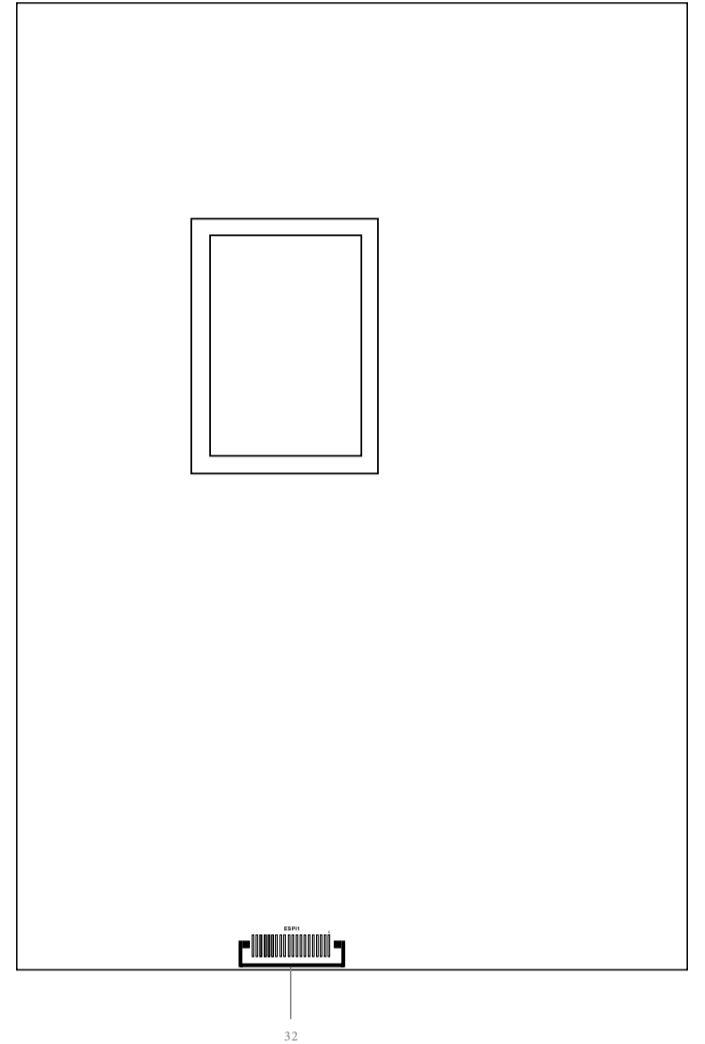
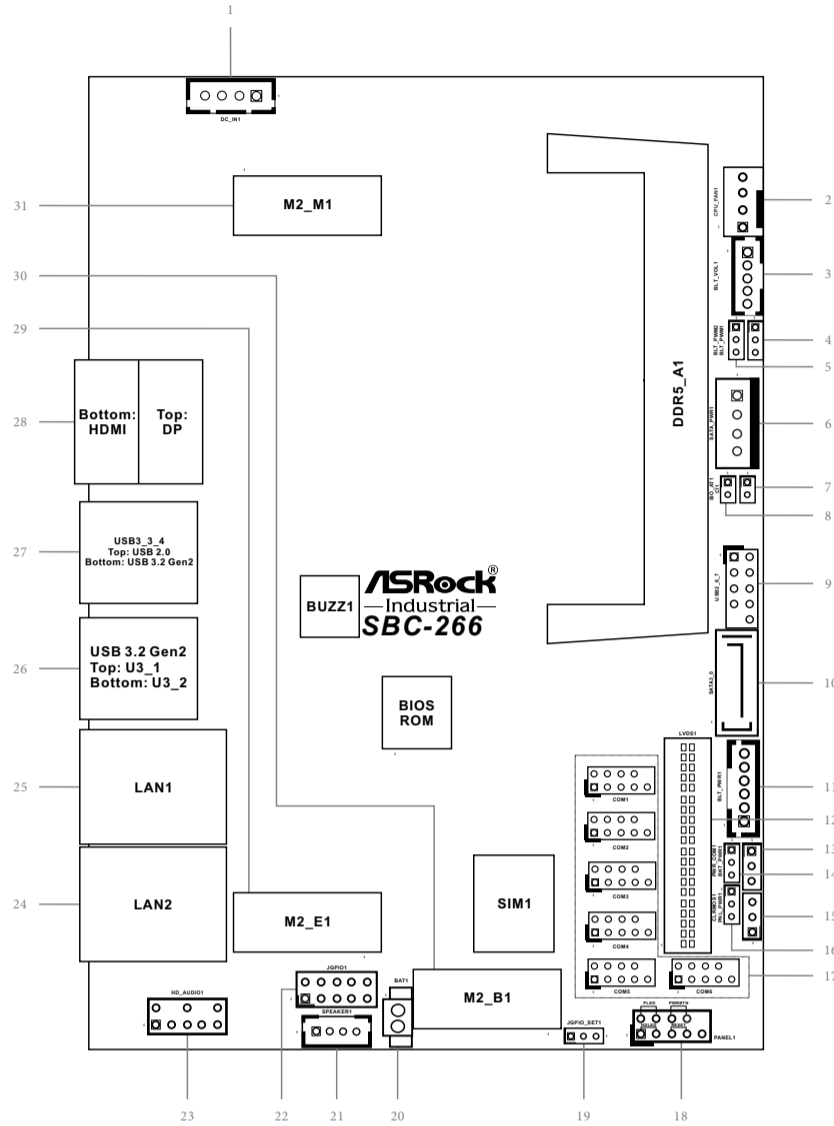
Bottom:

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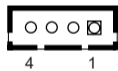
Revision History

Date	Description
February 13, 2026	First Release



1 : 4-pin DC-in PWR Connector (Input +9V~+36V) (DC-IN1)

Pin	Signal Name
1	GND
2	DC Input
3	DC Input
4	GND



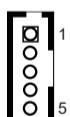
2 : CPU FAN Connector (+12V) (CPU_FAN1)

Pin	Signal Name
1	GND
2	+12V
3	CPU_FAN_SPEED
4	FAN_SPEED_CONTROL



3 : Backlight Volume Control (BLT_VOL1)

Pin	Signal Name
1	PWRDN
2	BLUP
3	BLDN
4	GND
5	GND



4 : Brightness Control Mode (BLT_PWM1)
1-2 : From eDP PWM to CON_LBKLT_CTL
2-3 : From LVDS PWM to CON_LBKLT_CTL (Default)

- Please set to 1-2 when adjusting brightness by Brightness Control bar under OS.
- Please set to 2-3 when adjusting brightness by BLT_VOL1.



5 : CON_LBKLT_CTL Voltage Level (BLT_PWM2)
1-2 : 3V Level (Default)
2-3 : 5V Level



6 : SATA Power Output Connector (SATA_PWR1)

Pin	Signal Name
1	+5V
2	GND
3	GND
4	+12V



7 : Chassis Intrusion Header (CI1)
Open : Normal (Default)
Short : Active Case Open

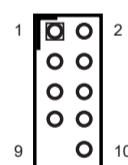


8 : ATX/AT Mode Jumper (SIO_AT1)
Open : ATX Mode (Default)
Short : AT Mode



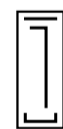
9 : USB 2.0 Connector (USB2_6_7)

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	USB_PWR	2
3	P-	P-	4
5	P+	P+	6
7	GND	GND	8
9		DUMMY	10



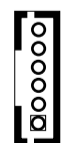
10 : SATA3 Connector (SATA3_0)

Pin	Signal Name
1	GND
2	SATA-A+
3	SATA-A-
4	GND
5	SATA-B-
6	SATA-B+
7	GND



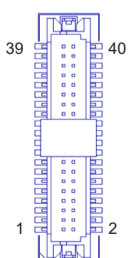
11 : Inverter Power Control Wafer (BLT_PWR1)

Pin	Signal Name
1	GND
2	GND
3	BL_CTL
4	BL_EN
5	LCD_BLT_VCC
6	LCD_BLT_VCC



12 : LVDS Panel Connector (LVDS1)

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	+3.3V	NA	4
5	NA	LVDS_A_DATA0#	6
7	LVDS_A_DATA0	GND	8
9	LVDS_A_DATA1#	LVDS_A_DATA1	10
11	GND	LVDS_A_DATA2#	12
13	LVDS_A_DATA2	GND	14
15	LVDS_A_DATA3#	LVDS_A_DATA3	16
17	GND	LVDS_A_CLK#	18
19	LVDS_A_CLK	GND	20
21	LVDS_B_DATA0#	LVDS_B_DATA0	22
23	GND	LVDS_B_DATA1#	24
25	LVDS_B_DATA1	GND	26
27	LVDS_B_DATA2#	LVDS_B_DATA2	28
29	DPLVDD_EN	LVDS_B_DATA3#	30
31	LVDS_B_DATA3	NC	32
33	LVDS_B_CLK#	LVDS_B_CLK	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40



• eDP by pass mode pin definition:

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	NA	NA	4
5	NA	NA	6
7	NA	GND	8
9	EDP_TX1#	EDP_TX1	10
11	GND	EDP_TX0#	12
13	EDP_TX0	GND	14
15	NA	NA	16
17	GND	EDP_AUXN	18
19	EDP_AUXP	GND	20
21	NA	NA	22
23	GND	NA	24
25	NA	GND	26
27	NA	NA	28
29	DPLVDD_EN	NA	30
31	NA	GND	32
33	NA	NA	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40

13 : Backlight Power Select (LCD_BLT_VCC) (BKT_PWR1)
1-2 : LCD_BLT_VCC: +5V (Default)
2-3 : LCD_BLT_VCC: +12V



14 : COM Port PWR Setting Jumper PWR_COM1 (For COM Port1)
Open : +0V
1-2 : +5V (Default)
2-3 : +12V



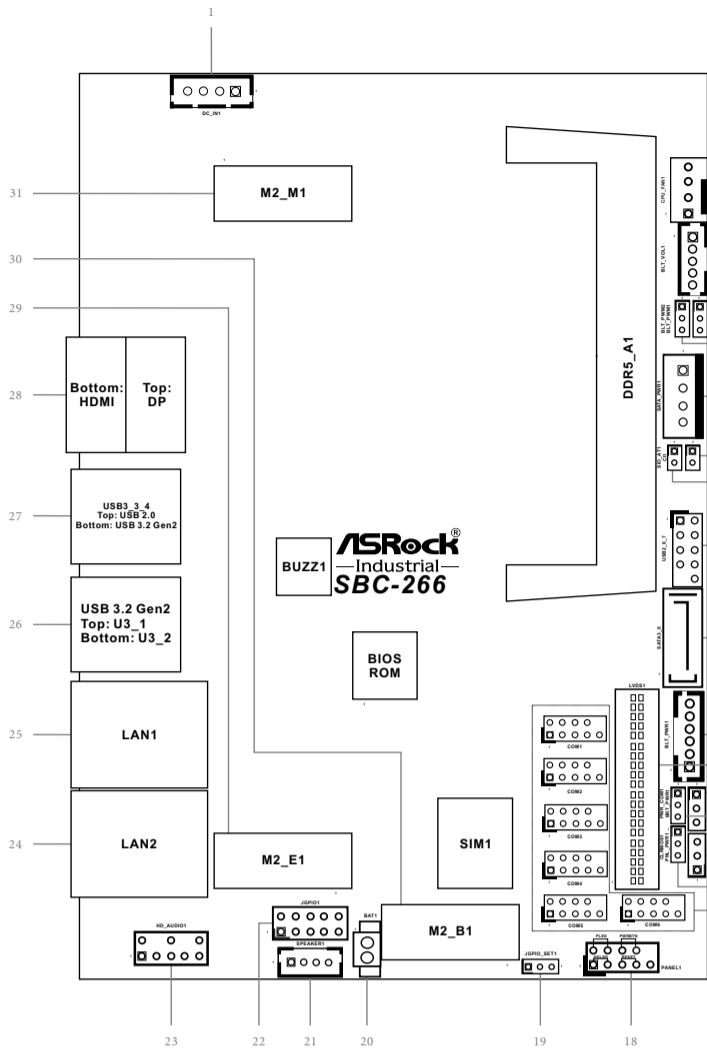
15 : Panel Power Select (LCD_VCC) (PNL_PWR1)
1-2 : +3V (Default)
2-3 : +5V



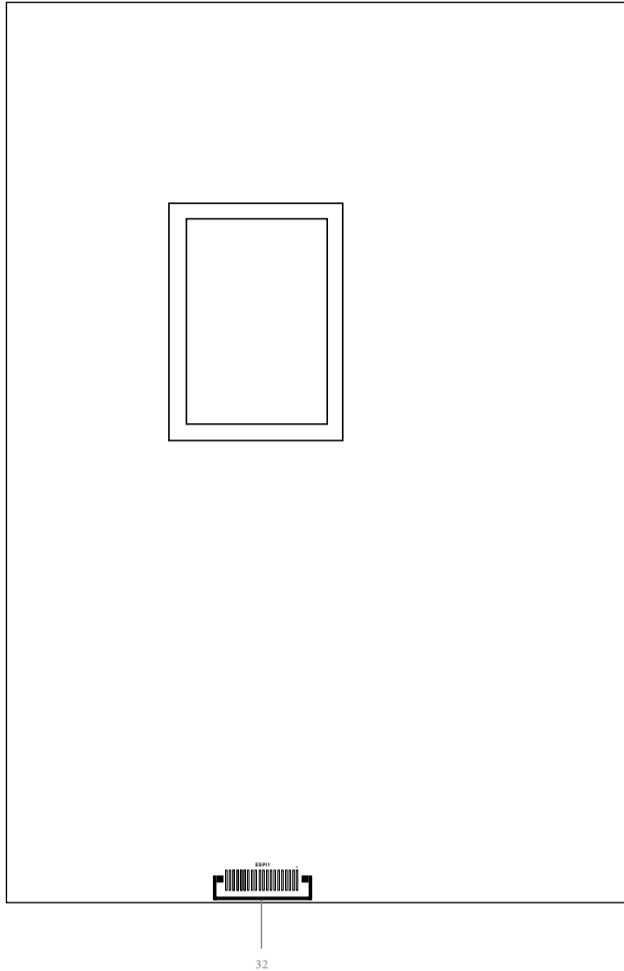
16 : Clear CMOS Header (CLRMO1)
1-2 : CLRMO2:
Auto Clear CMOS (Power Off)
2-3 : Clear CMOS



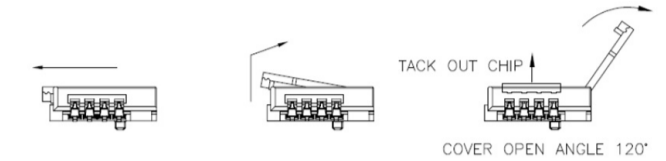
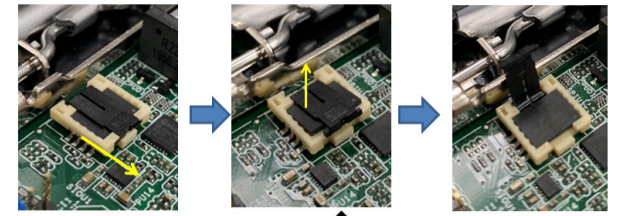
Top:



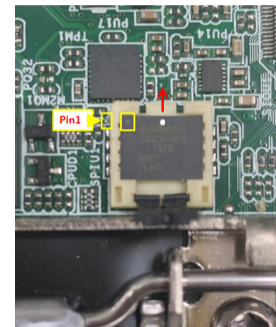
Bottom:



Installation of ROM Socket



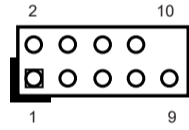
- Do not apply force to the actuator cover after IC inserted.
- Do not apply force to actuator cover when it is opening over 120 degrees. Otherwise, the actuator cover may be broken.



- The yellow dot (Pin1) on the ROM must be installed at Pin1 position of the socket (white arrow area).
 - Make sure the white dot on the ROM is installed outwards of the socket.
 - For further details of how to install ROM, please refer to ASRI website.
- Warning: If the installation does not follow as the picture, then it may cause severe damage to chipset & MB.**

17 : COM Port Headers COM1 (RS232/422/485)* COM2~COM6 (RS232)

Pin	Signal Name	Signal Name	Pin
1	DCCD#	RRXD	2
3	TTXD	DDTR#	4
5	GND	DDSR#	6
7	RRTS#	CCTS#	8
9	PWR		10



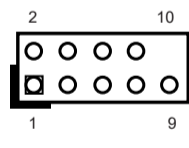
* This motherboard supports RS232/422/485 on COM1 port. Please refer to the table below for the pin definition. In addition, COM1 port (RS232/422/485) can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

COM1 Port Pin Definition

Pin	RS232	RS422	RS485
1	DCD	TX-	RTX-
2	RXD	TX+	RTX+
3	TXD	RX+	NA
4	DTR	RX-	NA
5	GND	GND	GND
6	DSR	NA	NA
7	RTS	NA	NA
8	CTS	NA	NA
9	PWR	PWR	PWR

18 : System Panel Header (PANEL1)

Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	GND		10



19 : GPIO Default Setting (JGPIO_SET1)

- 1-2 : Pull-High (Default)
- 2-3 : Pull-Low



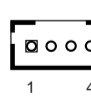
20 : Battery Connector (BAT1)

Pin	Signal Name
1	+BAT
2	GND



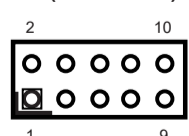
21 : 2W Audio AMP Output Wafer (SPEAKER1)

Pin	Signal Name
1	SPK L-
2	SPK L+
3	SPK R+
4	SPK R-



22 : Digital Input/Output Pin Header (JGPIO1)

Pin	Signal Name	Signal Name	Pin
1	GPP_A14	GPP_B15	2
3	GPP_A15	GPP_E1	4
5	GPP_A16	GPP_E2	6
7	GPP_A17	GPP_E3	8
9	+3V	GND	10

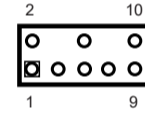


Parameter	Range
GPIO input Low voltage	Max: 0.8V
GPIO input High voltage	Low: 2V
GPIO output Low voltage	Max: 0.4V
GPIO output High voltage	Low: 2.4V

Note:
Max. load per GPIO pin: 3mA
Current Max. 1A per power pin.

23 : Front Panel Audio Header (HD_AUDIO1)

Pin	Signal Name	Signal Name	Pin
1	MIC1_L	GND	2
3	MIC1_R	MIC1_RET	4
5	OUT2_R		6
7	J_SENSE		8
9	OUT2_L	OUT_RET	10



24 : RJ45 1G LAN Port (LAN2)

25 : RJ45 1G LAN Port (LAN1)

26 : USB 3.2 Gen2 Ports (USB3_1_2)

Top : U3_1

Bottom : U3_2

27 : USB3_3_4

Top : USB 2.0 Port

Bottom : USB 3.2 Gen2 Port

28 : Top : DisplayPort (DP)

Bottom : HDMI Port (HDMI)

29 : M.2 Key-E Socket (M2_E1)

30 : M.2 Key-B Socket (M2_B1)

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	USB D+	+3.3V	4
5	USB D-	NA	6
7	GND	NA	8
9	CNV_WGR_D1-	CNV_RF_RESET	10
11	CNV_WGR_D1+	NA	12
13	GND	MODEM_CLKREQ	14
15	CNV_WGR_D0-	NA	16
17	CNV_WGR_D0+	GND	18
19	GND	NA	20
21	CNV_WGR_CLK-	CNV_BRI_RSP	22
23	CNV_WGR_CLK+		
		CNV_BGI_DT	32
33	GND	CNV_RGI_RSP	34
35	PETp	CNV_BRI_DT	36
37	PETn	NA	38
39	GND	NA	40
41	PERp0	NA	42
43	PERn	NA	44
45	GND	NA	46
47	PEFCLKp	NA	48
49	PEFCLKn	SUSCLK	50
51	GND	PERST0#	52
53	CLKREQ#	W_DISABLE1#	54
55	NA	W_DISABLE2#	56
57	GND	SMB_DATA	58
59	CNV_WT_D1-	SMB_CLK	60
61	CNV_WT_D1+	NA	62
63	GND	NA	64
65	CNV_WT_D0-	NA	66
67	CNV_WT_D0+	NA	68
69	GND	NA	70
71	CNV_WT_CLK-	+3.3V	72
73	CNV_WT_CLK+	+3.3V	74
75	GND		

Pin	Signal Name	Signal Name	Pin
1	NA	+3.3V	2
3	GND	+3.3V	4
5	GND	FuLL_Card Power off	6
7	USB D+	W_DISABLE	8
9	USB D-	NA	10
11	GND		
		NA	20
21	NA	NA	22
23	NA	NA	24
25	NA	W_DISABLE	26
27	GND	NA	28
29	NA	UIM_RESET	30
31	NA	UIM_CLK	32
33	GND	UIM_DATA	34
35	NA	UIM_PWR	36
37	NA	NA	38
39	GND	NA	40
41	PERn0	NA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETp0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
59	NA	NA	60
61	NA	NA	62
63	NA	NA	64
65	NA	NA	66
67	NA	NA	68
69	NA	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	NA		

31 : M.2 Key-M Socket (M2_M1)

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	NA	NA	6
7	NA	NA	8
9	GND	SATA_LED	10
11	NA	+3.3V	12
13	NA	+3.3V	14
15	GND	+3.3V	16
17	NA	+3.3V	18
19	NA	NA	20
21	GND	NA	22
23	NA	NA	24
25	NA	NA	26
27	GND	NA	28
29	NA	NA	30
31	NA	GND	32
33	GND	NA	34
35	NA	NA	36
37	NA	GND	38
39	GND	SMB_CLK	40
41	PERn0/SATA-B+	SMB_DATA	42
43	PERp0/SATA-B-	NA	44
45	GND	NA	46
47	PETn0/SATA-A-	NA	48
49	PETp0/SATA-A+	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
		NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

Backside :

32 : ESPI Connector (ESPI1)

Pin	Signal Name
1	GND
2	C_ESPI_CLK
3	GND
4	C_ESPI_CS#
5	DEBUG RESET
6	GND
7	+3V
8	GND
9	SMB_CLK MAIN
10	SMB_DATA MAIN
11	C_ESPI_IO0
12	C_ESPI_IO1
13	C_ESPI_IO2
14	C_ESPI_IO3
15	GND
16	+3VSB
17	N/A
18	N/A
19	C_ESPI_ALERT#
20	GND

