ASRock Industrial

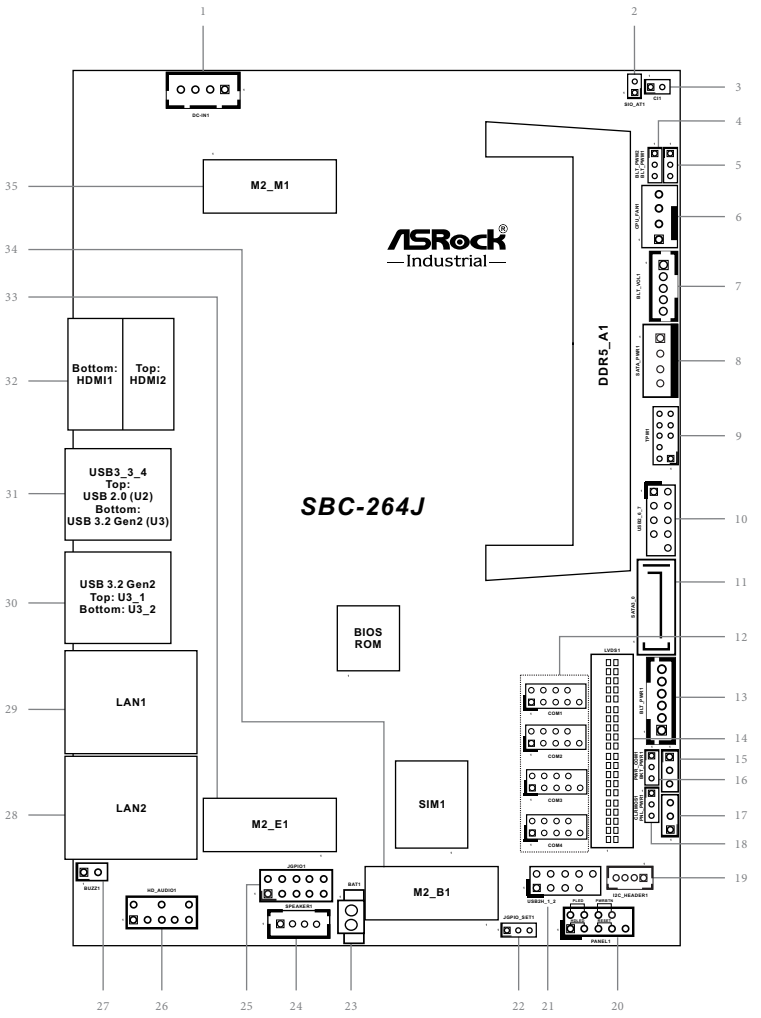
SBC-264J

Jumpers and Headers Setting Guide

Revision History

Date	Description
November 27, 2025	First Release
December 2, 2025	Second Release
January 15, 2026	Third Release
February 2, 2026	Fourth Release

Top:



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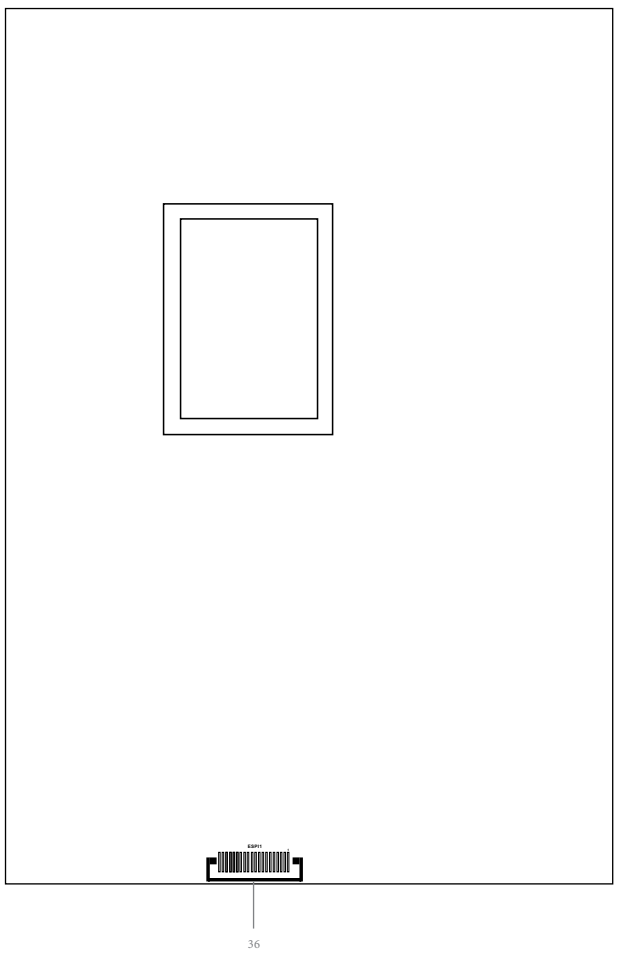
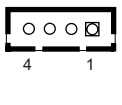


1 : 4-pin DC-in PWR Connector (Input +9V~+36V) (DC-IN1)

Pin	Signal Name
1	GND
2	DC Input
3	DC Input
4	GND



2 : ATX/AT Mode Jumper (SIO_AT1)

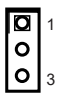
Open : ATX Mode (Default)
Close : AT Mode

3 : Chassis Intrusion Header (CI1)

Open : Normal (Default)
Close : Active Case Open

4 : CON_LBKLT_CTL Voltage Level (BLT_PWM2)

1-2 : 3V Level (Default)
2-3 : 5V Level



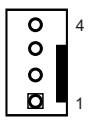
5 : Brightness Control Mode (BLT_PWM1)

1-2 : From eDP PWM to CON_LBKLT_CTL
2-3 : From LVDS PWM to CON_LBKLT_CTL (Default)

- Please set to 1-2 when adjusting brightness by Brightness Control bar under OS.
- Please set to 2-3 when adjusting brightness by BLT_VOL1.

6 : CPU FAN Connector (+12V) (CPU_FAN1)

Pin	Signal Name
1	GND
2	+12V
3	CPU_FAN_SPEED
4	FAN_SPEED_CONTROL

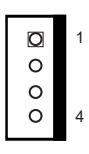


7 : Backlight Volume Control (BLT_VOL1)

Pin	Signal Name
1	PWRDN
2	BLUP
3	BLDN
4	GND
5	GND

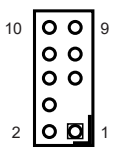
8 : SATA Power Output Connector (SATA_PWR1)

Pin	Signal Name
1	+5V
2	GND
3	GND
4	+12V



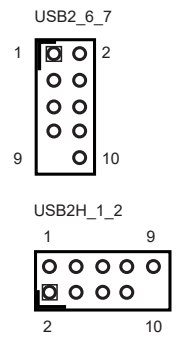
9 : TPM Header (TPM1)

Pin	Signal Name	Signal Name	Pin
1	TPM_PWR	RST#	2
3		CS#	4
5	IRA	MOSI	6
7	MISO	GND	8
9	CLK	GND	10



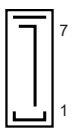
USB 2.0 Connectors
10 : USB2_6_7
21 : USB2H_1_2

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	USB_PWR	2
3	P-	P-	4
5	P+	P+	6
7	GND	GND	8
9		DUMMY	10



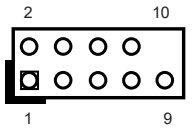
11 : SATA3 Connector (SATA3_0)

Pin	Signal Name
1	GND
2	SATA-A+
3	SATA-A-
4	GND
5	SATA-B-
6	SATA-B+
7	GND



12 : COM Port Headers
COM1 (RS232/422/485)*
COM2~COM4 (RS232)

Pin	Signal Name	Signal Name	Pin
1	DDCD#	RRXD	2
3	TTXD	DDTR#	4
5	GND	DDSR#	6
7	RRTS#	CCTS#	8
9	PWR		10



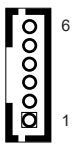
* This motherboard supports RS232/422/485 on COM1 port. Please refer to the table below for the pin definition. In addition, COM1 port (RS232/422/485) can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

COM1 Port Pin Definition

Pin	RS232	RS422	RS485
1	DCD	TX-	RTX-
2	RXD	TX+	RTX+
3	TXD	RX+	NA
4	DTR	RX-	NA
5	GND	GND	GND
6	DSR	NA	NA
7	RTS	NA	NA
8	CTS	NA	NA
9	PWR	PWR	PWR

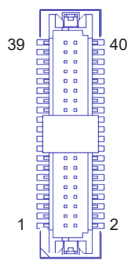
13 : Inverter Power Control Wafer (BLT_PWR1)

Pin	Signal Name
1	GND
2	GND
3	BL CTL
4	BL EN
5	LCD_BLT_VCC
6	LCD_BLT_VCC



14 : LVDS Panel Connector (LVDS1)

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	+3.3V	NA	4
5	NA	LVDS_A_DATA0#	6
7	LVDS_A_DATA0	GND	8
9	LVDS_A_DATA1#	LVDS_A_DATA1	10
11	GND	LVDS_A_DATA2#	12
13	LVDS_A_DATA2	GND	14
15	LVDS_A_DATA3#	LVDS_A_DATA3	16
17	GND	LVDS_A_CLK#	18
19	LVDS_A_CLK	GND	20
21	LVDS_B_DATA0#	LVDS_B_DATA0	22
23	GND	LVDS_B_DATA1#	24
25	LVDS_B_DATA1	GND	26
27	LVDS_B_DATA2#	LVDS_B_DATA2	28
29	DPLVDD_EN	LVDS_B_DATA3#	30
31	LVDS_B_DATA3	NC	32
33	LVDS_B_CLK#	LVDS_B_CLK	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40

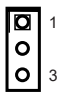


- eDP by pass mode pin definition:

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	NA	NA	4
5	NA	NA	6
7	NA	GND	8
9	EDP_TX1#	EDP_TX1	10
11	GND	EDP_TX0#	12
13	EDP_TX0	GND	14
15	NA	NA	16
17	GND	EDP_AUXN	18
19	EDP_AUXP	GND	20
21	NA	NA	22
23	GND	NA	24
25	NA	GND	26
27	NA	NA	28
29	DPLVDD_EN	NA	30
31	NA	GND	32
33	NA	NA	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40

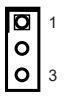
15 : Backlight Power Select (LCD_BLT_VCC) (BKT_PWR1)

1-2 : LCD_BLT_VCC: +5V (Default)
2-3 : LCD_BLT_VCC: +12V

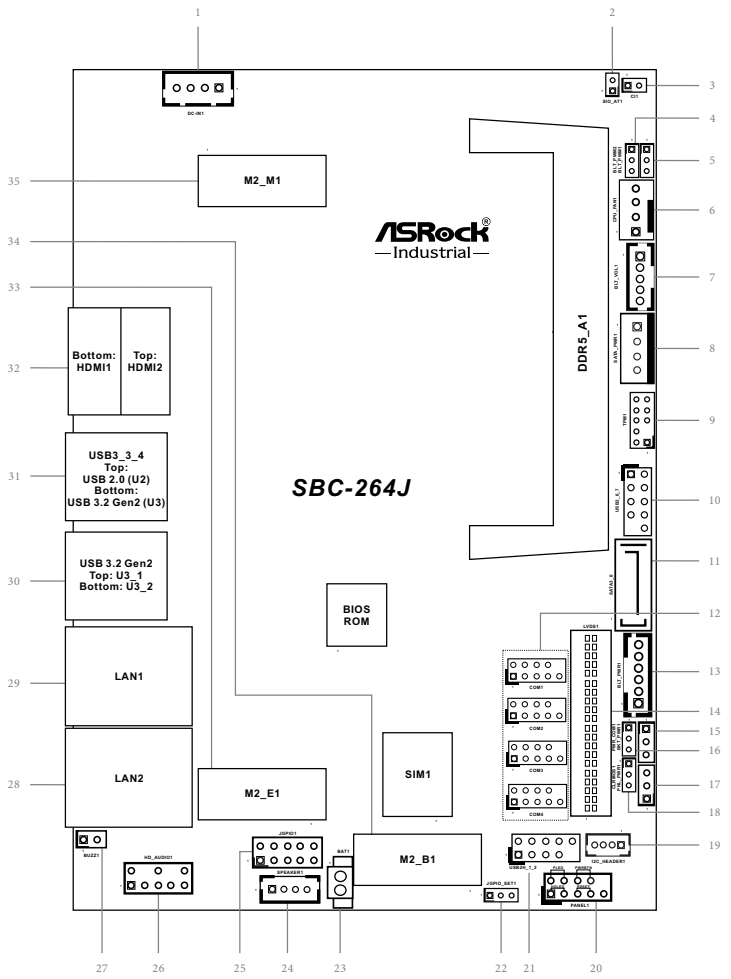


16 : COM Port PWR Setting Jumper PWR_COM1 (For COM Port1)

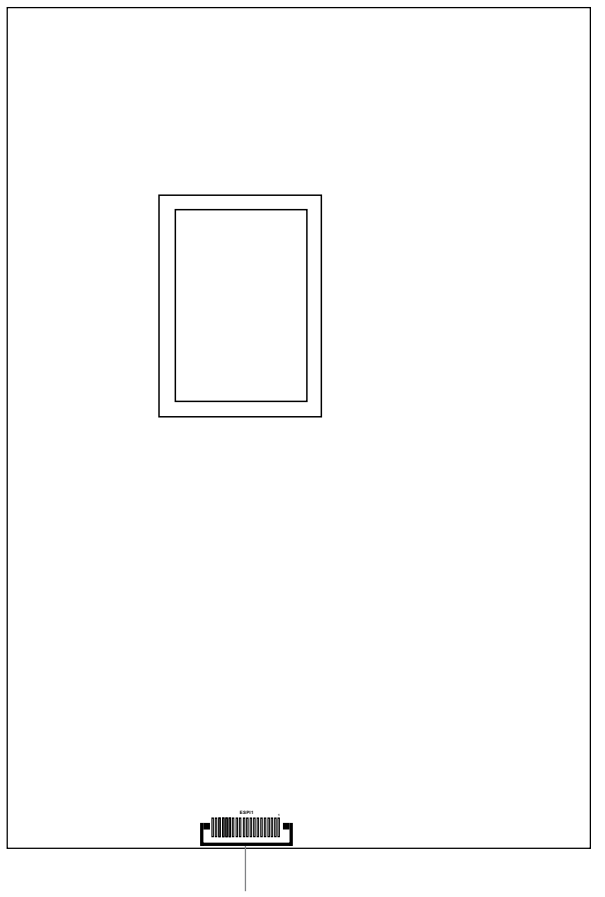
Open : +0V
1-2 : +5V (Default)
2-3 : +12V



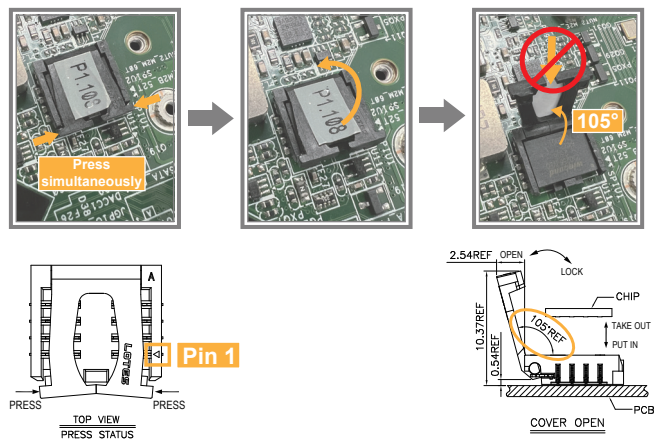
Top:



Bottom:



Installation of LOTES ROM Socket



- Do not press one side of the actuator cover at a time. Always apply even and simultaneous force to both sides to avoid damage.
- Do not apply force to the actuator cover after the IC is inserted, especially when it is fully opened at 105 degrees. Pressing vertically at this angle may cause the cover to break.

- The white dot (Pin 1) on the ROM must align with the Pin 1 position of the socket (white arrow area).
- Ensure the white dot on the ROM is facing outward from the socket.

Warning: Incorrect installation may damage the chipset and motherboard. Refer to the picture for proper orientation.

17 : Panel Power Select (LCD_VCC) (PNL_PWR1)

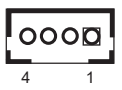
1-2 : +3V (Default)
2-3 : +5V

18 : Clear CMOS Header (CLRMOS1)

1-2 : CLRMOS2:
Auto Clear CMOS (Power Off)
2-3 : Clear CMOS

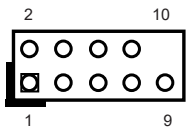
19 : I2C_HEADER1

Pin	Signal Name
1	+3V
2	I2C_CLK
3	I2C_DATA
4	GND



20 : System Panel Header (PANEL1)

Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	+5VSB		10

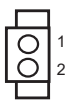


22 : GPIO Default Setting (JGPIO_SET1)

1-2 : Pull-High (Default)
2-3 : Pull-Low

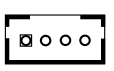
23 : Battery Connector (BAT1)

Pin	Signal Name
1	+BAT
2	GND



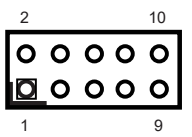
24 : 2W Audio AMP Output Wafer (SPEAKER1)

Pin	Signal Name
1	SPK L-
2	SPK L+
3	SPK R+
4	SPK R-



25 : Digital Input/Output Pin Header (JGPIO1)

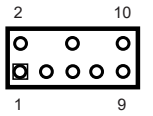
Pin	Signal Name	Signal Name	Pin
1	GPP_A14	GPP_B15	2
3	GPP_A15	GPP_E1	4
5	GPP_A16	GPP_E2	6
7	GPP_A17	GPP_E13	8
9	+3V	GND	10



Parameter	Range
GPIO input Low voltage	Max: 0.8V
GPIO input High voltage	Low: 2V
GPIO output Low voltage	Max: 0.4V
GPIO output High voltage	Low: 2.4V
Note: Max. load per GPI/O pin: 3mA Current Max. 1A per power pin.	

26 : Front Panel Audio Header (HD_AUDIO1)

Pin	Signal Name	Signal Name	Pin
1	MIC1_L	GND	2
3	MIC1_R		4
5	OUT2_R	MIC1_RET	6
7	J_SENSE		8
9	OUT2_L	OUT_RET	10



27 : Buzzer Header (BUZZ1)

Pin	Signal Name
1	+5V
2	BUZZ_LOW

28 : RJ45 2.5G LAN Port (LAN2)

29 : RJ45 2.5G LAN Port (LAN1)

30 : USB 3.2 Gen2 Ports (USB3_1_2)

Top : U3_1
Bottom : U3_2

31 : USB3_3_4

Top : USB 2.0 Port (U2)
Bottom : USB 3.2 Gen2 Port (U3)

32 : HDMI1_2

Top : HDMI Port (HDMI2)
Bottom : HDMI Port (HDMI1)

33 : M.2 Key-E Socket (M2_E1)

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	USB_D+	+3.3V	4
5	USB_D-	NA	6
7	GND	NA	8
9	CNV_WGR_D1-	CNV_RF_RESET	10
11	CNV_WGR_D1+	NA	12
13	GND	MODEM_ CLKREQ	14
15	CNV_WGR_D0-	NA	16
17	CNV_WGR_D0+	GND	18
19	GND	NA	20
21	CNV_WGR_CLK-	CNV_BRI_RSP	22
23	CNV_WGR_ CLK+		
		CNV_BGI_DT	32
33	GND	CNV_RGI_RSP	34
35	PETp	CNV_BRI_DT	36
37	PETn	NA	38
39	GND	NA	40
41	PERp	NA	42
43	PERn	NA	44
45	GND	NA	46
47	PEFCLKp	NA	48
49	PEFCLKn	SUSCLK	50
51	GND	PERST0#	52
53	CLKREQ#	W_DISABLE1#	54
55	NA	W_DISABLE2#	56
57	GND	SMB_DATA	58
59	CNV_WT_D1-	SMB_CLK	60
61	CNV_WT_D1+	NA	62
63	GND	NA	64
65	CNV_WT_D0-	NA	66
67	CNV_WT_D0+	NA	68
69	GND	NA	70
71	CNV_WT_CLK-	+3.3V	72
73	CNV_WT_CLK+	+3.3V	74
75	GND		

34 : M.2 Key-B Socket (M2_B1)

Pin	Signal Name	Signal Name	Pin
1	NA	+3.3V	2
3	GND	+3.3V	4
5	GND	FuLL_Card_ Power_off	6
7	USB_D+	W_DISABLE	8
9	USB_D-	NA	10
11	GND		
		NA	20
21	NA	NA	22
23	NA	NA	24
25	NA	W_DISABLE	26
27	GND	NA	28
29	NA	UIM_RESET	30
31	NA	UIM_CLK	32
33	GND	UIM_DATA	34
35	NA	UIM_PWR	36
37	NA	NA	38
39	GND	NA	40
41	PERn	NA	42
43	PERp	NA	44
45	GND	NA	46
47	PETn	NA	48
49	PETp	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
59	NA	NA	60
61	NA	NA	62
63	NA	NA	64
65	NA	NA	66
67	NA	NA	68
69	NA	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	NA		

35 : M.2 Key-M Socket (M2_M1)

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	NA	NA	6
7	NA	NA	8
9	GND	SATA_LED	10
11	NA	+3.3V	12
13	NA	+3.3V	14
15	GND	+3.3V	16
17	NA	+3.3V	18
19	NA	NA	20
21	GND	NA	22
23	NA	NA	24
25	NA	NA	26
27	GND	NA	28
29	NA	NA	30
31	NA	GND	32
33	GND	P+	34
35	NA	P-	36
37	NA	GND	38
39	GND	SMB_CLK	40
41	PERn0/SATA-B+	SMB_DATA	42
43	PERp0/SATA-B-	NA	44
45	GND	NA	46
47	PETn0/SATA-A-	NA	48
49	PETP0/SATA-A+	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

Backside :

36 : ESPI Connector (ESPI1)

Pin	Signal Name
1	GND
2	C_ESPI_CLK
3	GND
4	C_ESPI_CS#
5	DEBUG_RESET
6	GND
7	+3V
8	GND
9	SMB_CLK_MAIN
10	SMB_DATA_MAIN
11	C_ESPI_IO0
12	C_ESPI_IO1
13	C_ESPI_IO2
14	C_ESPI_IO3
15	GND
16	+3VSB
17	NA
18	NA
19	C_ESPI_ALERT#
20	GND