

NUCS-1360P/D4

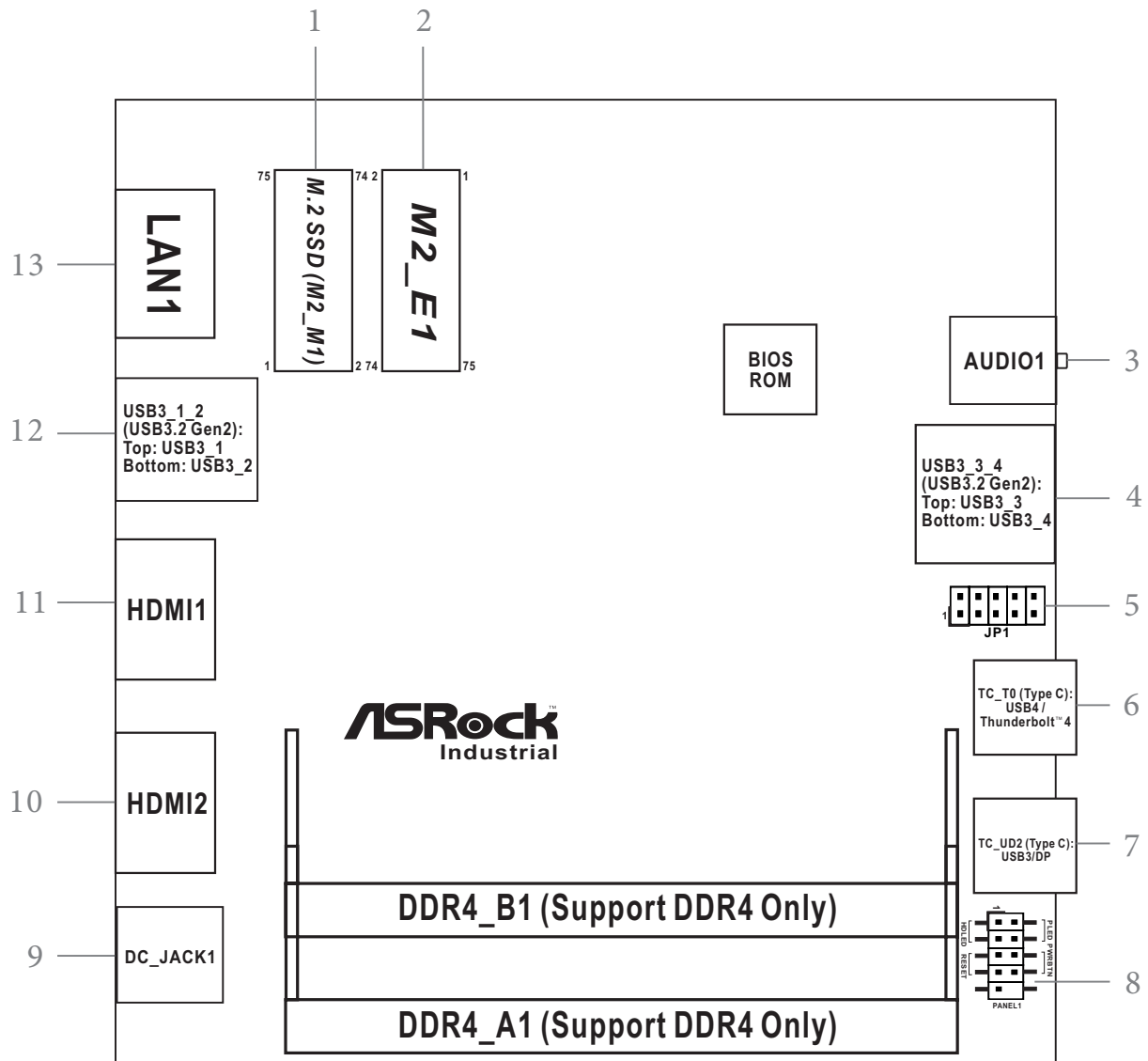
NUCS-1340P/D4

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Revision History

Date	Description
November 25, 2022	First Release
March 20, 2023	Second Release
January 19, 2024	Third Release



1 : M.2 Key-M Socket (M2_M1)

Pin	Signal Name	Signal Name	Pin
75	GND		
73	GND	+3.3V	74
71	GND	+3.3V	72
69	PEDET	+3.3V	70
67	NA	NA	68
57	GND	NA	58
55	PEFCLKp	NA	56
53	PEFCLKn	WAKE#	54
51	GND	CLKREQ#	52
49	PETP0	PERST#	50
47	PETn0	NA	48
45	GND	NA	46
43	PERp0	NA	44
41	PERn0	NA	42
39	GND	NA	40
37	PETp1	GND	38
35	PETn1	USB2_DN	36
33	GND	USB2_DP	34
31	PERp1	GND	32
29	PERn1	NA	30
27	GND	NA	28
25	PETp2	NA	26
23	PETn2	NA	24
21	GND	NA	22
19	PERp2	NA	20
17	PERn2	+3.3V	18
15	GND	+3.3V	16
13	PETp3	+3.3V	14
11	PETn3	+3.3V	12
9	GND	LED#	10
7	PERp3	NA	8
5	PERn3	NA	6
3	GND	+3.3V	4
1	GND	+3.3V	2

2 : M.2 Key-E Socket (M2_E1)

Pin	Signal Name	Signal Name	Pin
2	+3.3V	GND	1
4	+3.3V	USB_D+	3
6	NA	USB_D-	5
8	NA	GND	7
10	CNV_RF_RESET	CNV_WGR_D1-	9
12	NA	CNV_WGR_D1+	11
14	MODEM_CLKREQ	GND	13
16	NA	CNV_WGR_D0-	15
18	GND	CNV_WGR_D0+	17
20	NA	GND	19
22	CNV_BRI_RSP	CNV_WGR_CLK-	21
		CNV_WGR_CLK+	23
32	CNV_BGI_DT	GND	33
34	CNV_RGI_RSP	PETp	35
36	CNV_BRI_DT	PETn	37
38	NA	GND	39
40	NA	PERp	41
42	NA	PERn	43
44	NA	GND	45
46	NA	PEFCLKp	47
48	NA	PEFCLKn	49
50	SUSCLK	GND	51
52	PERST0#	CLKREQ#	53
54	W_DISABLE1#	WAKE#	55
56	W_DISABLE2#	GND	57
58	NA	CNV_WT_D1-	59
60	NA	CNV_WT_D1+	61
62	NA	GND	63
64	NA	CNV_WT_D0-	65
66	NA	CNV_WT_D0+	67
68	NA	GND	69
70	NA	CNV_WT_CLK-	71
72	+3.3V	CNV_WT_CLK+	73
74	+3.3V	GND	75

3 : Audio Jack (AUDIO1)

4 : USB 3.2 Gen2 Ports (USB3_3_4)

5 : JP1

- JP1_21: SIO AT Mode
- JP1_35: DACC*
- JP1_46: CMOS2
- JP1_68: CMOS

* Auto clear CMOS when system boot improperly.

6 : USB4/Thunderbolt™ 4 Type-C Port (TC_T0)

7 : USB3/DP Type-C Port (TC_UD2)

8 : System Panel Header (PANEL1)

Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	GND		10

9 : DC-In Jack (DC_JACK1)

10 : HDMI Port (HDMI2)

11 : HDMI Port (HDMI1)

12 : USB 3.2 Gen2 Ports (USB3_1_2)

13 : RJ-45 LAN Port (LAN1)

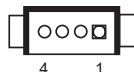
Back Side :

Power Button (PWR_BTN1)



Fan Connector (FAN1)

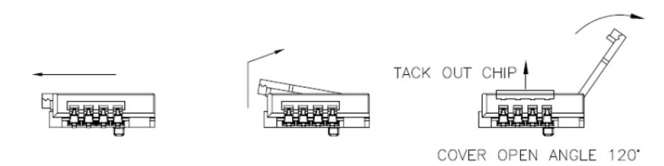
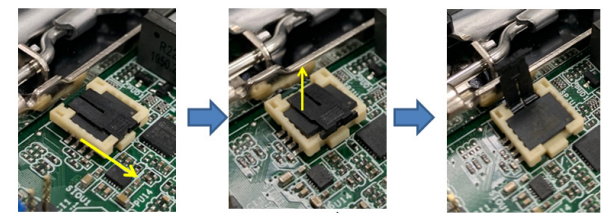
Pin	Signal Name
1	GND
2	+5V
3	FAN_SPEED
4	FAN_SPEED_CONTROL



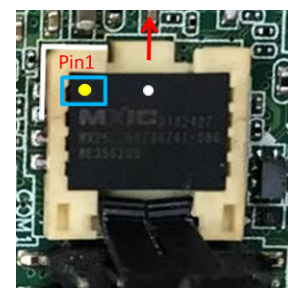
Battery Connector (BAT1)

ESPI Connector (ESPI1)

Installation of ROM Socket



* Do not apply force to the actuator cover after ic is inserted.
* Do not apply force to actuator cover when it is opening over 120 degree, Otherwise, the actuator cover may be broken.



* The yellow dot (Pin1) on the ROM must be installed at pin1 position of the socket.
* Make sure the white dot on the ROM is installed outwards of the socket.
* For further details of how to install ROM, please refer to ASRI website.
Warning: If the installation does not follow as the picture, then it may cause severe damage to chipset & MB.