# Jumpers and Headers Setting Guide

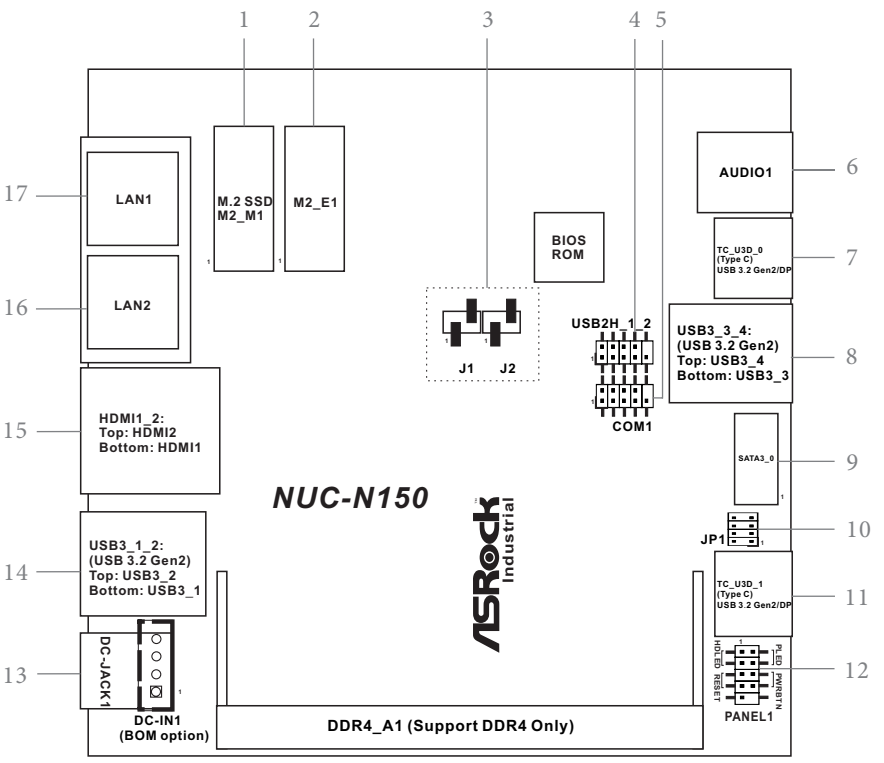
## NUC-N150



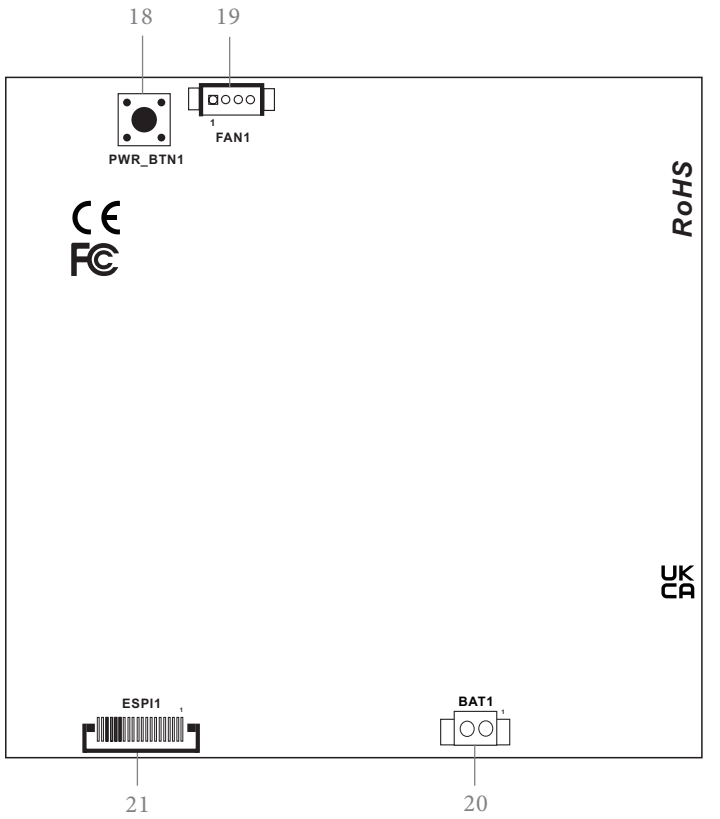
**Revision History**

| Date | Description |
|---|---|
| June 5, 2026 | First Release |

## Top:




## Bottom:




### 1 : M.2 Key-M Socket (M2_M1)

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | GND | +3.3V | 2 |
| 3 | GND | +3.3V | 4 |
| 5 | N/C | N/C | 6 |
| 7 | N/C | N/C | 8 |
| 9 | GND | LED# | 10 |
| 11 | N/C | +3V | 12 |
| 13 | N/C | +3V | 14 |
| 15 | GND | +3V | 16 |
| 17 | N/C | +3V | 18 |
| 19 | N/C | N/C | 20 |
| 21 | GND | N/C | 22 |
| 23 | N/C | N/C | 24 |
| 25 | N/C | N/C | 26 |
| 27 | GND | N/C | 28 |
| 29 | N/C | N/C | 30 |
| 31 | N/C | N/C | 32 |
| 33 | GND | USB_D+ | 34 |
| 35 | N/C | USB_D- | 36 |
| 37 | N/C | N/C | 38 |
| 39 | GND | SMB_CLK | 40 |
| 41 | PERn0/SATA-B+ | SMB_DATA | 42 |
| 43 | PERp0/SATA-B- | N/C | 44 |
| 45 | GND | N/C | 46 |
| 47 | PETn0/SATA-A- | N/C | 48 |
| 49 | PETp0/SATA-A+ | PERST# | 50 |
| 51 | GND | CLKREQ# | 52 |
| 53 | REFCLKn | WAKE# | 54 |
| 55 | REFCLKp | N/C | 56 |
| 57 | GND | N/C | 58 |
| | | | |
| 67 | N/C | SUSCLK | 68 |
| 69 | PEDET | +3.3V | 70 |
| 71 | GND | +3.3V | 72 |
| 73 | GND | +3.3V | 74 |
| 75 | GND | N/C | 76 |
| 77 | N/C | N/C | 78 |
| 79 | N/C | | |

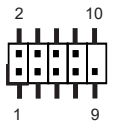
### 2 : M.2 Key-E Socket (M2_E1)

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | GND | +3.3V | 2 |
| 3 | USB_D+ | +3.3V | 4 |
| 5 | USB_D- | NA | 6 |
| 7 | GND | NA | 8 |
| 9 | CNV_WGR_D1- | CNV_RF_RESET | 10 |
| 11 | CNV_WGR_D1+ | NA | 12 |
| 13 | GND | MODEM_ CLKREQ | 14 |
| 15 | CNV_WGR_D0- | NA | 16 |
| 17 | CNV_WGR_D0+ | GND | 18 |
| 19 | GND | NA | 20 |
| 21 | CNV_WGR_CLK- | CNV_BRI_RSP | 22 |
| 23 | CNV_WGR_CLK+ | | |
| | | | |
| 33 | GND | CNV_BGI_DT | 32 |
| 35 | PETp | CNV_RGI_RSP | 34 |
| 37 | PETn | CNV_BRI_DT | 36 |
| 39 | GND | NA | 38 |
| 41 | PERp | NA | 40 |
| 43 | PERn | NA | 42 |
| 45 | GND | NA | 44 |
| 47 | PEFCLKp | NA | 46 |
| 49 | PEFCLKn | NA | 48 |
| 51 | GND | SUSCLK | 50 |
| 53 | CLKREQ# | PERST0# | 52 |
| 55 | WAKE# | W_DISABLE1# | 54 |
| 57 | GND | W_DISABLE2# | 56 |
| 59 | CNV_WT_D1- | SMB_DATA | 58 |
| 61 | CNV_WT_D1+ | SMB_CLK | 60 |
| 63 | GND | NA | 62 |
| 65 | CNV_WT_D0- | | 64 |
| 67 | CNV_WT_D0+ | NA | 66 |
| 69 | GND | NA | 68 |
| 71 | CNV_WT_CLK- | NA | 70 |
| 73 | CNV_WT_CLK+ | +3.3V | 72 |
| 75 | GND | +3.3V | 74 |

### 3 : J1, J2 Headers
(SMT type, 2-pin headers)
M.2 Key-M USB 2.0 function
Short : Enabled
Open : Disabled

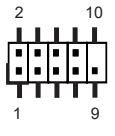

### 4 : USB 2.0 Connector (USB2H_1_2)

| Pin | Signal Name | Signal Name | Pin |
|---|---|---|---|
| 1 | USB_PWR | USB_PWR | 2 |
| 3 | -A | -B | 4 |
| 5 | +A | +B | 6 |
| 7 | GND | GND | 8 |
| 9 | DUMMY | | 10 |




### 5 : COM Port Header (COM1) (RS-232/422/485)*

| Pin | Signal Name | Signal Name | Pin |
|---|---|---|---|
| 1 | DDCD#1 | RRXD1 | 2 |
| 3 | TTXD1 | DDTR#1 | 4 |
| 5 | GND | DDSR#1 | 6 |
| 7 | RRTS#1 | CCTS#1 | 8 |
| 9 | DUMMY | | 10 |




* This motherboard supports RS232/422/485 on COM1 port. Please refer to the table below for the pin definition. In addition, COM1 port (RS232/422/485) can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

**COM1 Port Pin Definition**

| Pin | RS232 | RS422 | RS485 |
|---|---|---|---|
| 1 | DCD | TX- | RTX- |
| 2 | RXD | TX+ | RTX+ |
| 3 | TXD | RX+ | NA |
| 4 | DTR | RX- | NA |
| 5 | GND | GND | GND |
| 6 | DSR | NA | NA |
| 7 | RTS | NA | NA |
| 8 | CTS | NA | NA |
| 9 | NA | NA | NA |

### 6 : Audio Jack (AUDIO1)

### 7 : USB 3.2 Gen2/DP Type-C Port (TC_U3D_0)

### 8 : USB 3.2 Gen2 Ports (USB3_3_4)

### 9 : SATA3 Port (SATA3_0)

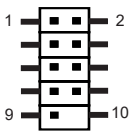
### 10 : JP1
1-2 : SIO AT Mode
(Default Open: SIO ATX Mode)
4-6 : Clear CMOS
3-4 : Auto Clear CMOS
5-7 : DACC*


• Auto clear CMOS when system boot improperly.

### 11 : USB 3.2 Gen2/DP Type-C Port (TC_U3D_1)

### 12 : System Panel Header (PANEL1)

| Pin | Signal Name | Signal Name | Pin |
|---|---|---|---|
| 1 | HDLED+ | PLED+ | 2 |
| 3 | HDLED- | PLED- | 4 |
| 5 | GND | PWRBTN# | 6 |
| 7 | RESET# | GND | 8 |
| 9 | GND | | 10 |




### 13 : DC-In Jack (DC_JACK1)
4-pin DC-in Wafer (DC_IN1) -- BOM option
1-4 : GND
2-3 : DC Input


### 14 : USB 3.2 Gen2 Ports (USB3_1_2)

### 15 : HDMI Ports (HDMI1_2)

### 16 : RJ-45 LAN Port (LAN2)

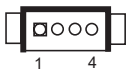
### 17 : RJ-45 LAN Port (LAN1)

Back Side :

### 18 : Power Button (PWR_BTN1)

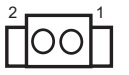
### 19 : Fan Connector (FAN1)

| Pin | Signal Name |
|---|---|
| 1 | GND |
| 2 | +5V |
| 3 | FAN_SPEED |
| 4 | FAN_SPEED_CONTROL |




### 20 : Battery Connector (BAT1)

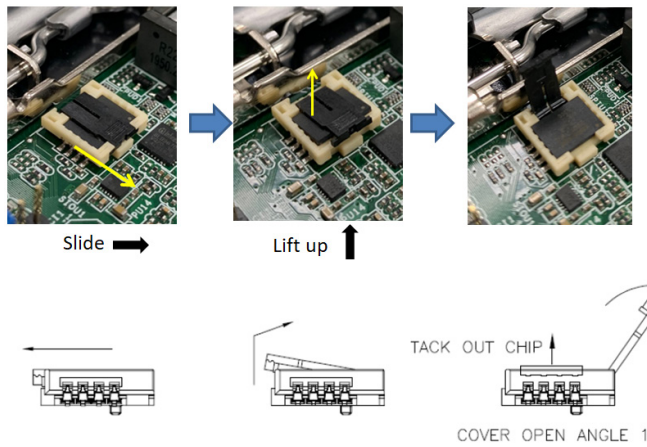
| Pin | Signal Name |
|---|---|
| 1 | +BAT |
| 2 | GND |



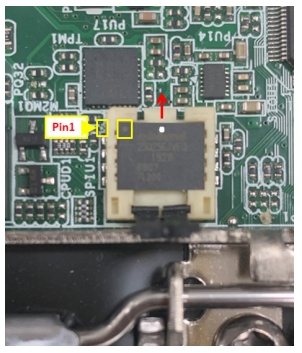

### 21 : ESPI Connector (ESPI)

| Pin | Signal Name |
|---|---|
| 1 | GND |
| 2 | ESPI_CLK |
| 3 | GND |
| 4 | ESPI_CS# |
| 5 | ESPI_RESET# |
| 6 | GND |
| 7 | +3V |
| 8 | GND |
| 9 | SMB_CLK |
| 10 | SMB_DATA |
| 11 | ESPI_IO0 |
| 12 | ESPI_IO1 |
| 13 | ESPI_IO2 |
| 14 | ESPI_IO3 |
| 15 | GND |
| 16 | +3VSB |
| 17 | Internal use |
| 18 | Internal use |
| 19 | ESPI_ALERT# |
| 20 | GND |

## Installation of ACES ROM Socket



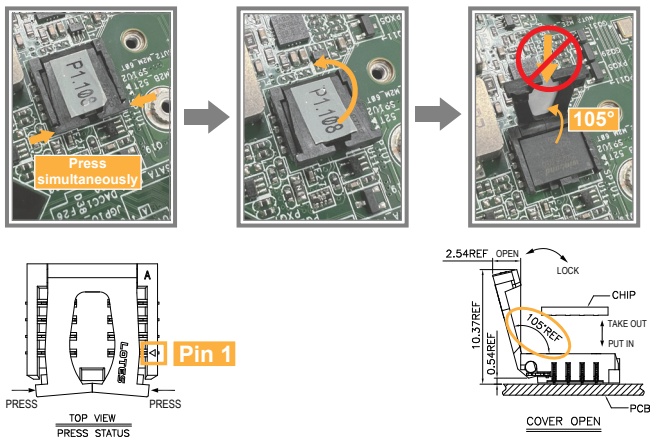

- Do not apply force to the actuator cover after the IC is inserted.
- Do not apply force to actuator cover when it is opening over 120 degrees. Otherwise, the actuator cover may break.




- The white dot (Pin 1) on the ROM must align with the Pin 1 position of the socket (white arrow area).
- Ensure the white dot on the ROM is facing outward from the socket.

**Warning: Incorrect installation may damage the chipset and motherboard. Refer to the picture for proper orientation.**

## Installation of LOTES ROM Socket




- Do not press one side of the actuator cover at a time. Always apply even and simultaneous force to both sides to avoid damage.
- Do not apply force to the actuator cover after the IC is inserted, especially when it is fully opened at 105 degrees. Pressing vertically at this angle may cause the cover to break.


- The white dot (Pin 1) on the ROM must align with the Pin 1 position of the socket (white arrow area).
- Ensure the white dot on the ROM is facing outward from the socket.

**Warning: Incorrect installation may damage the chipset and motherboard. Refer to the picture for proper orientation.**