Jumpers and Headers Setting Guide

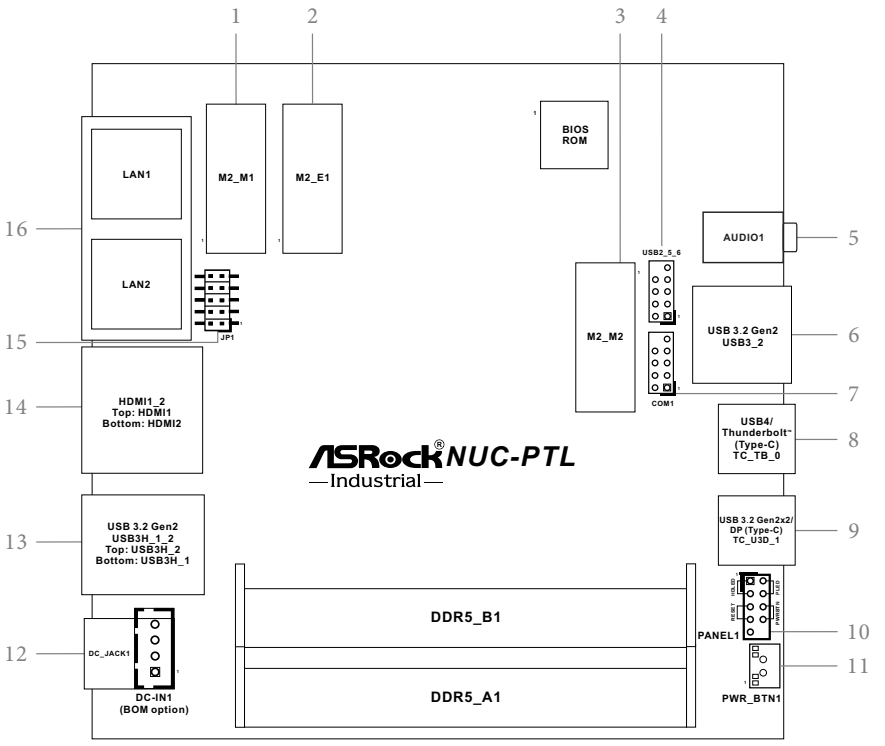
NUC-358H

NUC-325

Revision History

Date	Description
June 19, 2025	First Release
July 31, 2025	Second Release
September 11, 2025	Third Release
January 20, 2026	Fourth Release

Top:



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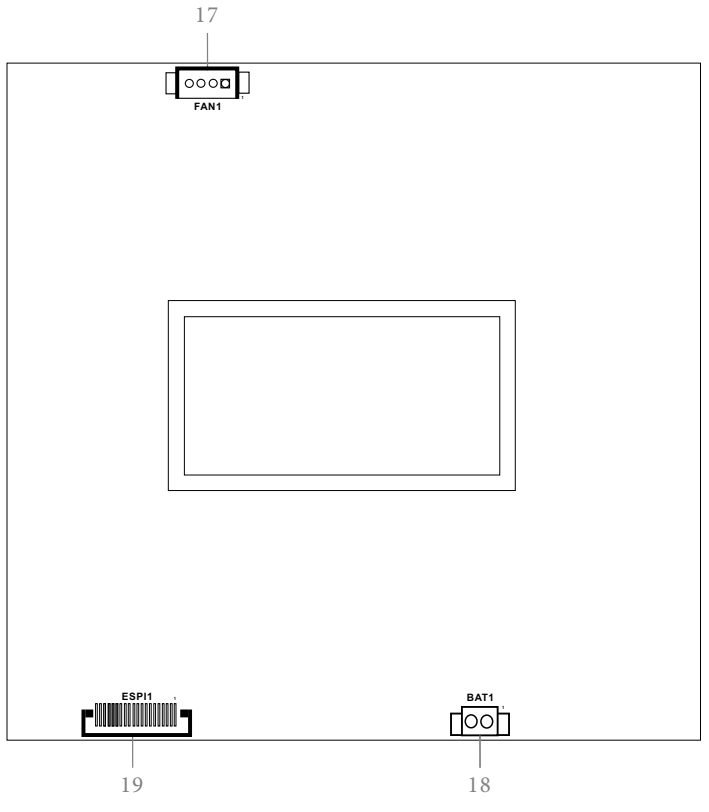


1 : M.2 Key-M Socket (M2_M1)

Pin	Signal	Signal	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	PERn3	NA	6
7	PERp3	NA	8
9	GND	HDLED	10
11	PETn3	+3.3V	12
13	PETp3	+3.3V	14
15	GND	+3.3V	16
17	PERn2	+3.3V	18
19	PERp2	NA	20
21	GND	NA	22
23	PETn2	NA	24
25	PETp2	NA	26
27	GND	NA	28
29	PERn1	NA	30
31	PERp1	GND	32
33	GND	USB_D+	34
35	PETn1	USB_D-	36
37	PETp1	GND	38
39	GND	NA	40
41	PERn0	NA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETP0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	NA	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

2 : M.2 Key-E Socket (M2_E1)

Pin	Signal	Signal	Pin
1	GND	+3.3V	2
3	USB_D+	+3.3V	4
5	USB_D-	NA	6
7	GND	NA	8
9	CNV_WGR_D1-	CNV_RF_RESET	10
11	CNV_WGR_D1+	NA	12
13	GND	MODEM_ CLKREQ	14
15	CNV_WGR_D0-	NA	16
17	CNV_WGR_D0+	GND	18
19	GND	NA	20
21	CNV_WGR_CLK-	CNV_BRI_RSP	22
23	CNV_WGR_CLK+		
		CNV_BGI_DT	32
33	GND	CNV_RGI_RSP	34
35	PETp	CNV_BRI_DT	36
37	PETn	NA	38
39	GND	NA	40
41	PERp	NA	42
43	PERn	NA	44
45	GND	NA	46
47	PEFCLKp	NA	48
49	PEFCLKn	NA	50
51	GND	PERST0#	52
53	CLKREQ#	W_DISABLE1#	54
55	NA	W_DISABLE2#	56
57	GND	NA	58
59	CNV_WT_D1-	NA	60
61	CNV_WT_D1+	NA	62
63	GND	NA	64
65	CNV_WT_D0-	NA	66
67	CNV_WT_D0+	NA	68
69	GND	NA	70
71	CNV_WT_CLK-	+3.3V	72
73	CNV_WT_CLK+	+3.3V	74
75	GND		

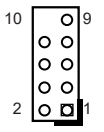
* Pin34 and Pin36 are defined as USB 2.0 signal to support Key-M to Key-B extension card.

3 : M.2 Key-M Socket (M2_M2)

Pin	Signal	Signal	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	PERn3	NA	6
7	PERp3	NA	8
9	GND	HDLED	10
11	PETn3	+3.3V	12
13	PETp3	+3.3V	14
15	GND	+3.3V	16
17	PERn2	+3.3V	18
19	PERp2	NA	20
21	GND	NA	22
23	PETn2	NA	24
25	PETp2	NA	26
27	GND	NA	28
29	PERn1	NA	30
31	PERp1	NA	32
33	GND	NA	34
35	PETn1	NA	36
37	PETp1	NA	38
39	GND	NA	40
41	PERn0	NA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETP0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	NA	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

4 : USB 2.0 Header (USB2_5_6)

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	USB_PWR	2
3	-A	-B	4
5	+A	+B	6
7	GND	GND	8
9	DUMMY		10

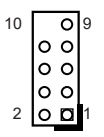


5 : Combo Audio Jack (AUDIO1) (Headphone + MIC)

6 : USB 3.2 Gen2 Port (USB3_2)

7 : COM Port Header (RS232/422/485) (COM1)

Pin	Signal Name	Signal Name	Pin
1	DDCD#1	RRXD1	2
3	TTXD1	DDTR#1	4
5	GND	DDSR#1	6
7	RRTS#1	CCTS#1	8
9	DUMMY		10



* This motherboard supports RS232/422/485 on COM1 port. Please refer to the table below for the pin definition. In addition, COM1 port (RS232/422/485) can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

COM1 Port Pin Definition

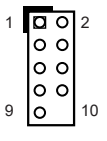
Pin	RS232	RS422	RS485
1	DCD	TX-	RTX-
2	RXD	TX+	RTX+
3	TXD	RX+	NA
4	DTR	RX-	NA
5	GND	GND	GND
6	DSR	NA	NA
7	RTS	NA	NA
8	CTS	NA	NA
9	NA	NA	NA

8 : USB4/Thunderbolt™ Type-C Port (TC_TB_0)

9 : USB 3.2 Gen2x2/DP Type-C Port (TC_U3D_1)

10 : System Panel Header (PANEL1)

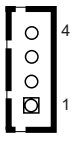
Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	+5VSB		10



11 : Power Button (PWR_BTN1)

12 : DC-In Jack (DC_JACK1)
4-pin DC-in Wafer (DC_IN1) (BOM option)

Pin	Signal Name
1	GND
2	DC Input
3	DC Input
4	GND



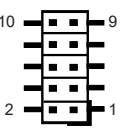
13 : USB 3.2 Gen2 Ports (USB3H_1_2)

14 : HDMI Ports (HDMI1_2)

15 : JP1 Header (JP1)

JP1_12 : Short : ATX Mode (Default)
JP1_12 : Open : AT Mode
JP1_34 : CMOS Normal (Default)
JP1_46 : Short : Clear CMOS
JP1_57 : Short : DACC* (Default)
JP1_910 : Short: Active Case Open

* Auto clear CMOS when system boot improperly.



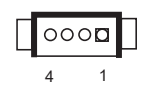
16 : RJ-45 LAN Ports

Left: LAN1
Right: LAN2

Back Side :

17 : Fan Connector (FAN1)

Pin	Signal Name
1	GND
2	+5V
3	FAN_SPEED
4	FAN_SPEED_CONTROL



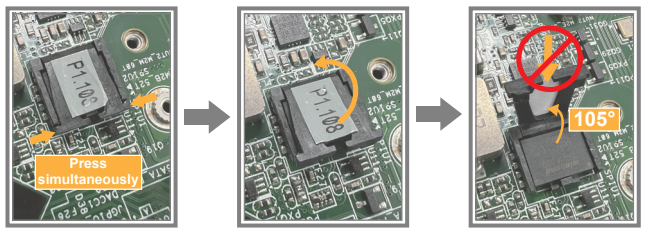
18 : Battery Connector (BAT1)

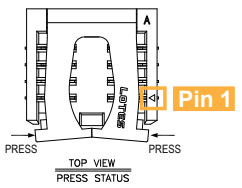
Pin	Signal Name
1	+BAT
2	GND

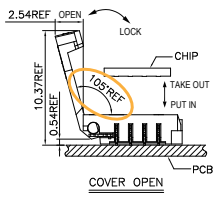
19 : ESPI Connector (ESPI)

Pin	Signal Name
1	GND
2	ESPI_CLK
3	GND
4	ESPI_CS#
5	ESPI_RESET#
6	GND
7	+3V
8	NA
9	SMB_CLK
10	SMB_DATA
11	ESPI_IO0
12	ESPI_IO1
13	ESPI_IO2
14	ESPI_IO3
15	NA
16	+3VSB
17	NA
18	NA
19	NA
20	GND

Installation of LOTES ROM Socket







- Do not press one side of the actuator cover at a time. Always apply even and simultaneous force to both sides to avoid damage.
- Do not apply force to the actuator cover after the IC is inserted, especially when it is fully opened at 105 degrees. Pressing vertically at this angle may cause the cover to break.

- The white dot (Pin 1) on the ROM must align with the Pin 1 position of the socket (white arrow area).
- Ensure the white dot on the ROM is facing outward from the socket.

Warning: Incorrect installation may damage the chipset and motherboard. Refer to the picture for proper orientation.