

IMB-X1904

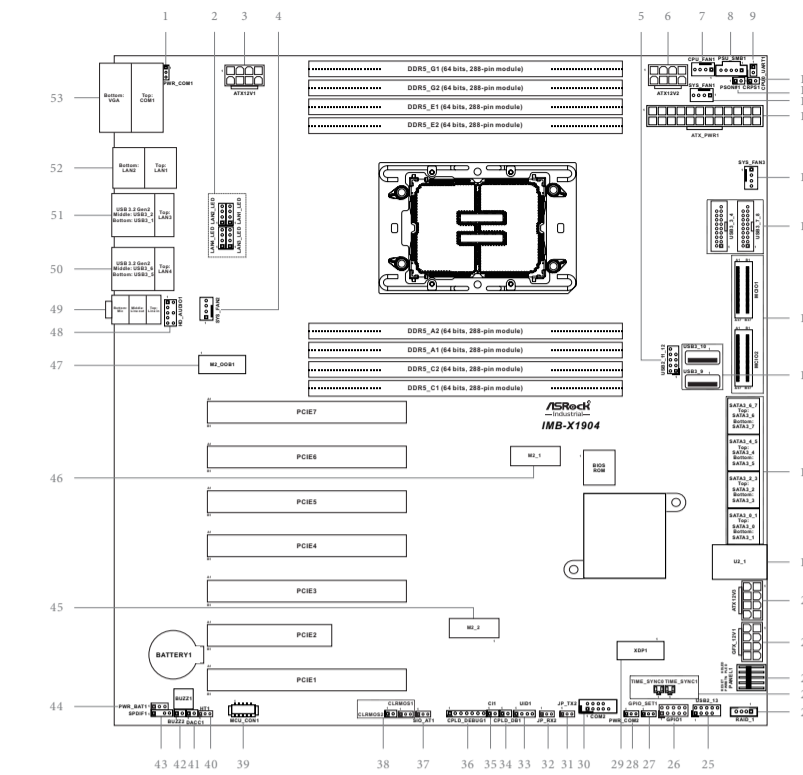
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Revision History

Date	Description
July 24, 2025	First Release
December 18, 2025	Second Release
February 3, 2026	Third Release
March 19, 2026	Fourth Release
April 17, 2026	Fifth Release

Jumpers and Headers Setting Guide



COM Port PWR Setting Jumpers

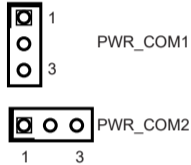
1 : PWR_COM1 (For COM Port1)

28 : PWR_COM2 (For COM Port2)

Open: +0V

1-2: +5V (Default)

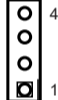
2-3: +12V



2 : LAN LED Headers (LAN1_LED, LAN2_LED, LAN3_LED, LAN4_LED)

LAN1_LED:

Pin	Signal Name
1	+3V_AUX
2	ALED1_ACT
3	ALED0_100
4	ALED2_1000



LAN2_LED:

Pin	Signal Name
1	+V3P3_LAN_JVL
2	LAN2_ACT
3	LAN2_100
4	LAN2_1000



LAN3_LED:

Pin	Signal Name
1	+3V_AUX
2	E610_SDP02_ACT
3	E610_SDP01_Others
4	E610_SDP00_10G



LAN4_LED:

Pin	Signal Name
1	+3V_AUX
2	E610_SDP06_ACT
3	E610_SDP05_Others
4	E610_SDP04_10G

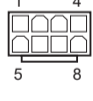


8-pin ATX 12V Power Connectors

3 : ATX12V1

6 : ATX12V2

Pin	Signal Name	Signal Name	Pin
1	GND	GND	2
3	GND	GND	4
5	ATX12V	ATX12V	6
7	ATX12V	ATX12V	8



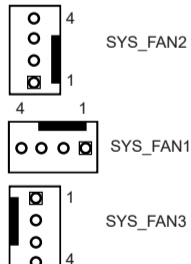
SYS FAN Connectors

4 : SYS_FAN2

12 : SYS_FAN1

14 : SYS_FAN3

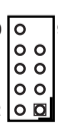
Pin	Signal Name
1	GND
2	SYS_FAN_VOUT
3	SYS_FAN_IN
4	SYS_FAN_PWMOUT



USB 2.0 Headers

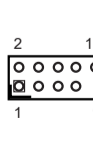
5 : USB2_11_12

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	USB_PWR	2
3	USB2 D-	USB2 D-	4
5	USB2 D+	USB2 D+	6
7	GND	GND	8
9		NA	10



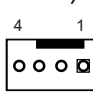
25 : USB2_13

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	NA	2
3	USB2 D-	NA	4
5	USB2 D+	NA	6
7	GND	NA	8
9		NA	10



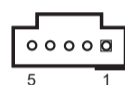
7 : CPU FAN Connector (CPU_FAN1)

Pin	Signal Name
1	GND
2	+12V
3	CPU_FAN_IN
4	CPU_FAN_OUT



8 : PSU_SMB1

Pin	Signal Name
1	SMB_CLK
2	SMB_DATA
3	SMB_ALERT#
4	GND
5	+3V



9 : CPU0_UART1

Pin	Signal Name
1	CPU0_UART_TXD_LVC3
2	CPU0_UART_RXD_LVC3



10 : CRPS1

Pin	Signal Name
1	ATX+5VSB
2	GND



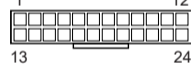
11 : PSON#1

Pin	Signal Name
1	PSON#
2	GND



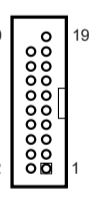
13 : 24-pin ATX Power Input Connector (ATXPWR1)

Pin	Signal Name	Signal Name	Pin
1	+3V	+3V	13
2	+3V	-12V	14
3	GND	GND	15
4	+5V	PSON#	16
5	GND	GND	17
6	+5V	GND	18
7	GND	GND	19
8	PWROK_PS	NA	20
9	+5VSB	+5V	21
10	ATX 24pin +12V	+5V	22
11	ATX 24pin +12V	+5V	23
12	+3V	GND	24



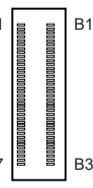
15 : USB 3.2 Gen1 Headers (USB3_3_4, USB3_7_8)

Pin	Signal Name	Signal Name	Pin
1	NA	USB2 D+	2
3	USB2 D+	USB2 D-	4
5	USB2 D-	GND	6
7	GND	SSTX+	8
9	SSTX+	SSTX-	10
11	SSTX-	GND	12
13	GND	SSRX+	14
15	SSRX+	SSRX-	16
17	SSRX-	USB_PWR	18
19	USB_PWR		20



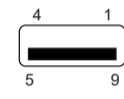
16 : MCIO Connectors (MCIO1, MCIO2)

Pin	Signal Name	Signal Name	Pin
A1	GND	GND	B1
A2	RX 0+	TX 0+	B2
A3	RX 0-	TX 0-	B3
A4	GND	GND	B4
A5	RX 1+	TX 1+	B5
A6	RX 1-	TX 1-	B6
A7	GND	GND	B7
A8	NA	SMB_CLK	B8
A9	WAKE#	SMB_DATA	B9
A10	GND	GND	B10
A11	CLK1+	PRST1	B11
A12	CLK1-	PRST1	B12
A13	GND	GND	B13
A14	RX 2+	TX 2+	B14
A15	RX 2-	TX 2-	B15
A16	GND	GND	B16
A17	RX 3+	TX 3+	B17
A18	RX 3-	TX 3-	B18
A19	GND	GND	B19
A20	RX 4+	TX 4+	B20
A21	RX 4-	TX 4-	B21
A22	GND	GND	B22
A23	RX 5+	TX 5+	B23
A24	RX 5-	TX 5-	B24
A25	GND	GND	B25
A26	NA	SMB_CLK	B26
A27	WAKE#	SMB_DATA	B27
A28	GND	GND	B28
A29	CLK2+	PRST2	B29
A30	CLK2-	PRST2	B30
A31	GND	GND	B31
A32	RX 6+	TX 6+	B32
A33	RX 6-	TX 6-	B33
A34	GND	GND	B34
A35	RX 7+	TX 7+	B35
A36	RX 7-	TX 7-	B36
A37	GND	GND	B37



17 : USB 3.2 Gen1 Header (Vertical Type-A) (USB3_9, USB3_10)

Pin	Signal Name
1	USB_PWR
2	USB2 D-
3	USB2 D+
4	GND
5	SSRX-
6	SSRX+
7	GND
8	SSTX-
9	SSTX+



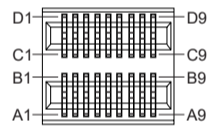
18 : SATA3 Connectors (SATA3_0~SATA7)

Pin	Signal Name
1	GND
2	SATA-A+
3	SATA-A-
4	GND
5	SATA-B-
6	SATA-B+
7	GND



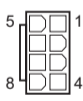
19 : U2_1

Pin	Signal Name	Signal Name	Pin
A1	PCIE CLK+	U2_RST#	B1
A2	PCIE CLK-	NA	B2
A3	GND	GND	B3
A4	RX1+	RX0+	B4
A5	RX1-	RX0-	B5
A6	GND	GND	B6
A7	RX3+	RX2+	B7
A8	RX3-	RX2-	B8
A9	GND	GND	B9



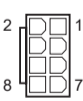
20 : 8-pin ATX 12V Power Connector (ATX12V3)

Pin	Signal Name	Signal Name	Pin
1	GND	GND	2
3	GND	GND	4
5	ATX12V	ATX12V	6
7	ATX12V	ATX12V	8



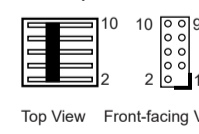
21 : 8-pin ATX_PCIE Power Connector (GFX_12V1)

Pin	Signal Name	Signal Name	Pin
1	PCIE +12V	GND	2
3	PCIE +12V	GND	4
5	PCIE +12V	GND	6
7	GND	GND	8



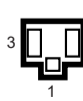
22 : System Panel Header (PANEL1)

Pin	Signal Name	Signal Name	Pin
1		GND	2
3	GND	RESET#	4
5	PWRBTN#	GND	6
7	PLED-	HDLED-	8
9	PLED+	HDLED+	10



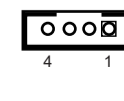
23 : TIME SYNC Headers (TIME_SYNC0, TIME_SYNC1)

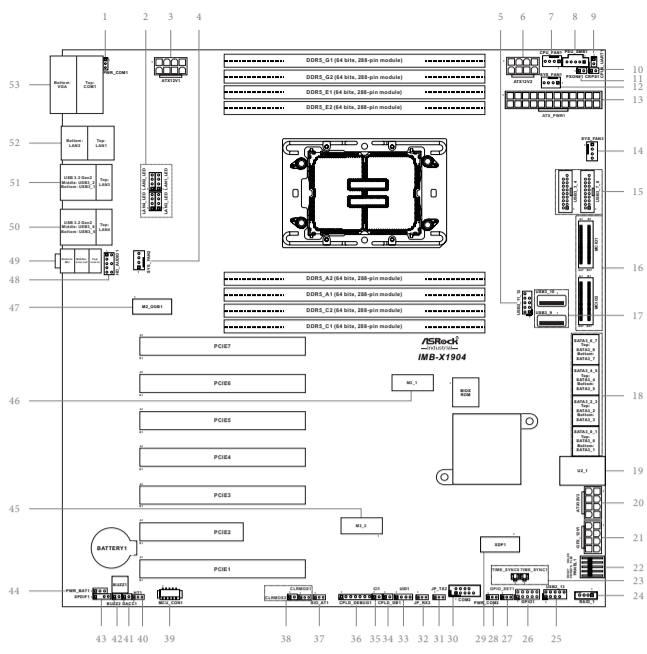
Pin	Signal Name
1	TIMED_GPIO
2	GND
3	GND



24 : RAID KEY (RAID_1)

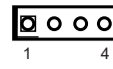
Pin	Signal Name
1	GND
2	PU_RAID_PIN2
3	GND
4	FM_VROC_RAID_KEY_R





33 : UID1

Pin	Signal Name
1	+5VSB
2	LOCATORLED-
3	FM_UID_BTN_N
4	GND



34 : CPLD_DB1

Pin	Signal Name
1	+3.3VSB_CPLD
2	FM_FORCE_PWRON_LVC3

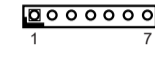


35 : Chassis Intrusion Header (CI1) Open : Normal (Default) Short : Active Case Open



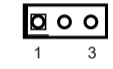
36 : CPLD_DEBUG1

Pin	Signal Name
1	+3.3VSB_CPLD
2	JTAG_PLD_TCK
3	JTAG_PLD_TDO
4	JTAG_PLD_TDI
5	JTAG_PLD_TDI_TRST_N
6	JTAG_PLD_TMS
7	GND



37 : ATX/AT Mode Jumper (SIO_AT1)

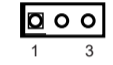
1-2 : AT Mode
2-3 : ATX Mode (Default)



38 : Clear CMOS Headers

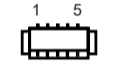
CLRMOSS1
1-2 : Normal (Default)
2-3 : Clear CMOS

CLRMOSS2
Open : Normal (Default)
Short : Auto Clear CMOS (Power Off)



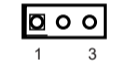
39 : MCU_CON1

Pin	Signal Name
1	+MCU_VDD
2	MCU_PSIN#
3	ICE_CLK_P5
4	MCU_RESET#
5	GND



40 : HEATER1 Header (HT1) (Preheat function)

Pin	Signal Name
1	Heater PWR (5V/1A)
2	GND
3	NTC (Negative Temperature Coefficient) thermistors



- The 10k Ohm NTC thermistor is suggested.
- Deep mode is not supported when the preheat function is enabled.

41 : DACC1

Open: no ACC
Short: ACC (Default)



- Auto clear CMOS when system boot improperly.

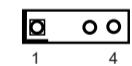
42 : Buzzer Header (BUZZ2)

Pin	Signal Name
1	+5V
2	BUZZ



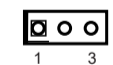
43 : SPDIF Header (SPDIF1)

Pin	Signal Name
1	+5V
2	NA
3	SPDIF OUT
4	GND



44 : PWR_BAT1

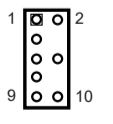
1-2 : Normal (Default)
2-3 : Charge Battery



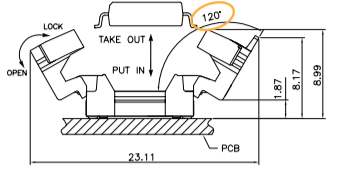
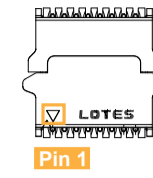
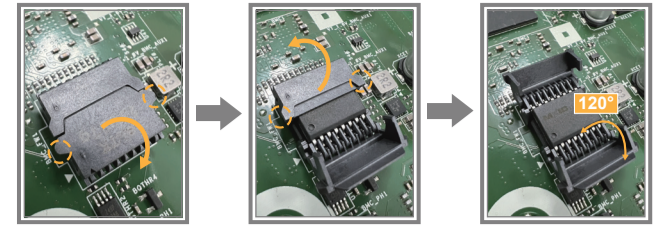
- Only supported by chargeable battery.

48 : Front Panel Audio Header (HD_AUDIO1)

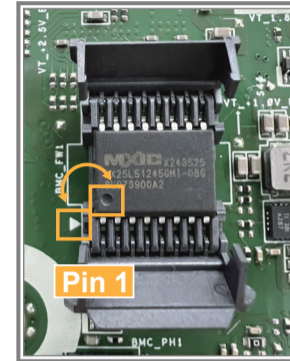
Pin	Signal Name	Signal Name	Pin
1	MIC2_L	GND	2
3	MIC2_R		4
5	OUT2_R	MIC_RET	6
7	J_SENSE		8
9	OUT2_L	OUT_RET	10



Installation of LOTES ROM Socket



Do not apply force to the actuator cover after the IC is inserted, especially when it is fully opened at 120 degrees. Pressing vertically at this angle may cause the cover to break.

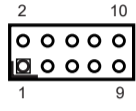


The black dot (Pin 1) on the ROM must align with the Pin 1 position of the socket (white arrow area). Ensure the black dot on the ROM is facing outward from the socket.

Warning: Incorrect installation may damage the chipset and motherboard. Refer to the picture for proper orientation.

26 : Digital Input/Output Pin Header (GPIO1)

Pin	Signal Name	Signal Name	Pin
1	GPP_E04_DO1	TIMED_GPIO0	2
3	GPP_E05_DO2	TIMED_GPIO1	4
5	GPP_E06_DO3	GPP_I02_DI3	6
7	GPP_E07_DO4	GPP_I03_DI4	8
9	+3V_DIO	GND	10



Parameter	Range
GPIO input Low voltage	Max: 0.8V
GPIO input High voltage	Min: 2.4V
GPIO output Low voltage	Max: 0.9V
GPIO output High voltage	Min: 2.5V

Note:
Max. load per GPIO pin: 3mA
Current Max. 1A per power pin

27 : Digital Input/Output Default Value

Setting (GPIO_SET1)
1-2: Pull-High (Default)
2-3: Pull-Low



29 : XDP1

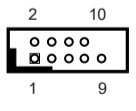
Pin	Net	Net	Pin
1	+1.05V_PCH	JTAG_DBP_TMS_R	2
3	JTAG_DBP_TCK	JTAG_DBP_TDO_R	4
5	JTAG_DBP_TDI_R	RST_DBP_RST_CO_N	6
7	DBP_PMODE	PD_TRST_PD3	8
9	JTAG_DBP_TRST	H_DBP_FREQ_N	10
11	H_DBP_PRDY_N	+1.05V_PCH	12
13	PCH_PTI_TRACE_CLK	GND	14
15	POD_PRSNT1_N	GND	16
17	POD_PRSNT2_N	NA	18
19	PCH_PTI_TRACE_D0	NA	20
21	PCH_PTI_TRACE_D1	NA	22
23	PCH_PTI_TRACE_D2	NA	24
25	PCH_PTI_TRACE_D3	NA	26
27	PCH_PTI_TRACE_D4	NA	28
29	PCH_PTI_TRACE_D5	NA	30
31	PCH_PTI_TRACE_D6	NA	32
33	PCH_PTI_TRACE_D7	NA	34
35	PCH_PTI_TRACE_D8	DBP_HOOK3_FBRK_N	36
37	PCH_PTI_TRACE_D9	DBP_HOOK2	38
39	PCH_PTI_TRACE_D10	DBP_POWER_BTN_BUF_N	40
41	PCH_PTI_TRACE_D11	FM_DBG_AUX_PWRGD_R	42
43	PCH_PTI_TRACE_D12	NA	44
45	PCH_PTI_TRACE_D13	NA	46
47	PCH_PTI_TRACE_D14	MB_DBP_STBY_LVC3_SCL	48
49	PCH_PTI_TRACE_D15	MB_DBP_STBY_LVC3_SDA	50
51	JTAG_DBP_PCH_R_TCK	+3VSB	52
53	DBP_CPU0_HOOK9_MBP3_N	NA	54
55	DBP_CPU0_HOOK8_MBP2_N	NA	56
57	GND	GND	58
59	GPP_F_17_M2_SKT2_CFG_2	GND	60

47 : M2_OOB1

Pin	Signal Name	Signal Name	Pin
1	GND	+3V_AUX	2
3	USB2_P14_DP_L	+3V_AUX	4
5	USB2_P14_DN_L	NA	6
7	GND	OOB_MOSI	8
9	NA	OOB_CS#	10
11	NA	OOB_SCLK	12
13	NA	OOB_MISO	14
15	NA	CPU0_OOB_SPI_SEL	16
17	NA	GPP_D20_DETECT	18
19	NA	NA	20
21	NA	OOB_TX	22
23	NA		
33	GND	NA	34
35	PCIE4_TXP_C	NA	36
37	PCIE4_TXN_C	NA	38
39	GND	SLP_S3#	40
41	PCIE4_RXP	RESETCON#	42
43	PCIE4_RXN	PWRBTN#	44
45	GND	CASEOPEN#	46
47	CLK_SRC7_DP	RTCSRST#	48
49	CLK_SRC7_DN	GPP_D22_HEARTBEAT	50
51	GND	S_PLTRST#	52
53	GND	NA	54
55	NA	NA	56
57	GND	OOB_SMB_DATA	58
59	NA	OOB_SMB_CLK	60
61	NA	GPP_D23_MPU_RESET	62
63	GND	GPP_D21_BOOT_SOURCE	64
65	NA	NA	66
67	NA	NA	68
69	GND	NA	70
71	NA	+3V_AUX	72
73	NA	+3V_AUX	74
75	GND		

30 : COM Port Header (COM2) (RS232)

Pin	Signal Name	Signal Name	Pin
1	DDCD#	RRXD	2
3	TTXD	DDTR#	4
5	GND	DDSR#	6
7	RRTS#	CCTS#	8
9	PWR		10



31 : JP_TX2

1-2 : TX to COM2 (Default)
2-3 : TX to M2_OOB1



32 : JP_RX2

1-2 : RX to COM2 (Default)
2-3 : RX to M2_OOB1



M.2 Key-M Sockets

45 : M2_2
46 : M2_1

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	PERn3	NA	6
7	PERp3	NA	8
9	GND	LED#	10
11	PETn3	+3.3V	12
13	PETp3	+3.3V	14
15	GND	+3.3V	16
17	PERn2	+3.3V	18
19	PERp2	NA	20
21	GND	NA	22
23	PETn2	NA	24
25	PETp2	NA	26
27	GND	NA	28
29	PERn1	NA	30
31	PERp1	NA	32
33	GND	NA	34
35	PETn1	NA	36
37	PETp1	NA	38
39	GND	SMB_CLK	40
41	PERn0	SMB_DATA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETp0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	SUSCLK	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

49 : Audio Jacks

Top: Blue: Line in
Middle: Green: Line out
Bottom: Pink: Mic

50 : Top : RJ45 LAN Port (LAN4)

Middle: USB 3.2 Gen2 Port (USB3_6)
Bottom: USB 3.2 Gen2 Port (USB3_5)

51 : Top : RJ45 LAN Port (LAN3)

Middle: USB 3.2 Gen2 Port (USB3_2)
Bottom: USB 3.2 Gen2 Port (USB3_1)

52 : Top : RJ45 LAN Port (LAN1)

Bottom: RJ45 LAN Port (LAN2)

53 : Top : COM Port (COM1) (RS232)

Bottom : D-Sub Port (VGA1)

Recommended Memory Configuration:

DIMM Card	A1	A2	C1	C2	E1	E2	G1	G2
1	V					V		
2			V		V			
4	V		V		V		V	
8	V	V	V	V	V	V	V	V

* The symbol "V" indicates the slot is populated.