Jumpers and Headers Setting Guide

ASRock Industrial

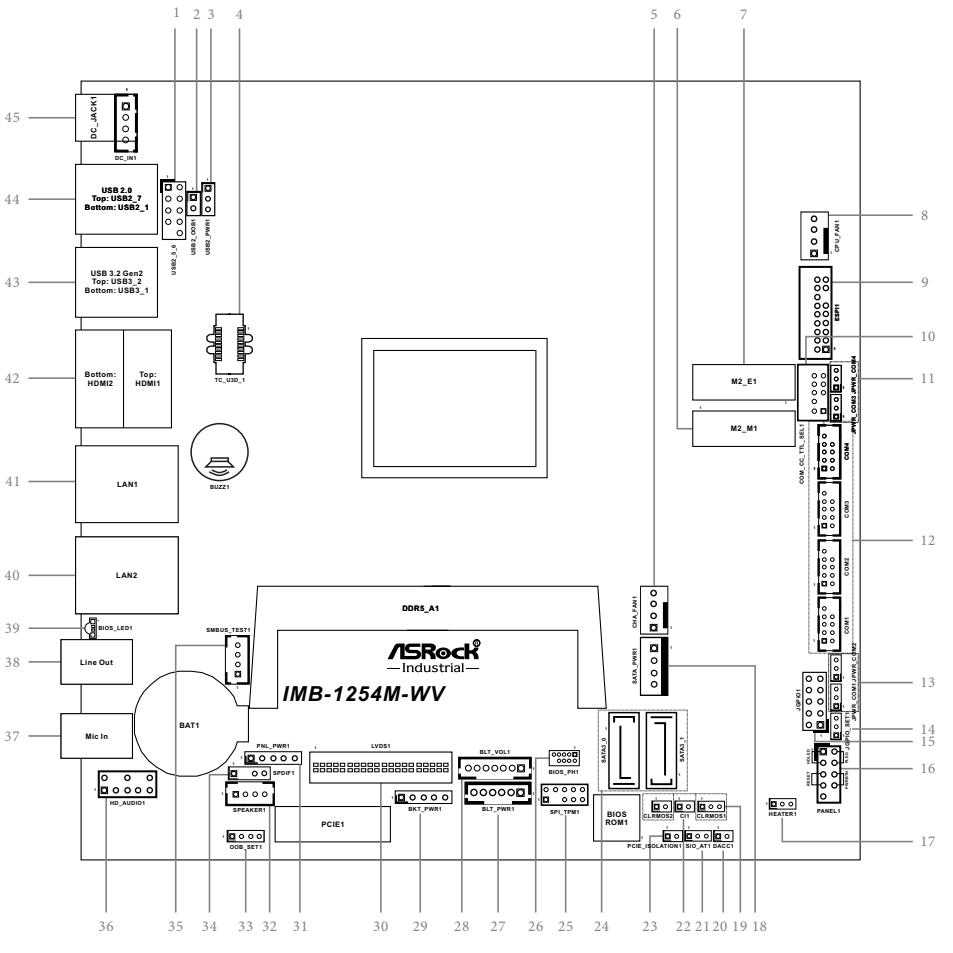
IMB-1254M-WV

IMB-1254E-WV

HDMI® HIGH-DEFINITION MULTIMEDIA INTERFACE

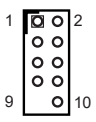
Revision History

Date	Description
April 1, 2026	First Release
June 11, 2026	Second Release
July 17, 2026	Third Release
July 30, 2026	Third Release



1 : USB 2.0 Header (USB2_5_6)

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	USB_PWR	2
3	USB_D-	USB_D-	4
5	USB_D+	USB_D+	6
7	GND	GND	8
9		DUMMY	10



2 : USB2_OOB1 (Onboard OOB only)

Pin	Signal Name
1	short USB2_5_6 Pin 4
2	short USB2_5_6 Pin 6

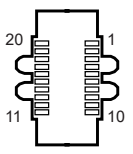
• Short Pin1&2 to share USB Port 6 signal of USB2_5_6 Header to OOB.

3 : USB2_5_6 POWER (USB2_PWR1)

1-2 : +5V
2-3 : +5VSB (Default)

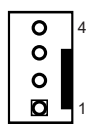
4 : Front Panel Type-C USB 3.2 Gen1 Header (TC_U3D_1)

Pin	Signal Name	Signal Name	Pin
10	SBU2	USB_PWR	11
9	SBU1	TX2+	12
8	CC1	TX2-	13
7	USB_PWR	GND	14
6	RX1-	RX2+	15
5	RX1+	RX2-	16
4	GND	GND	17
3	TX-	USB_D-	18
2	TX+	USB_D+	19
1	USB_PWR	CC2	20



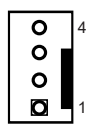
5 : Chassis FAN Connector (+12V) (CHA_FAN1)

Pin	Signal Name
1	GND
2	+12V
3	CHA_FAN_SPEED
4	FAN_SPEED_CONTROL



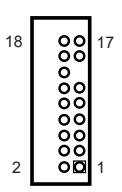
8 : CPU FAN Connector (+12V) (CPU_FAN1)

Pin	Signal Name
1	GND
2	+12V
3	CPU_FAN_SPEED
4	FAN_SPEED_CONTROL



9 : ESPI Header (ESPI1)

Pin	Signal Name	SiSignal Name	Pin
1	ESPI_CLK	GND	2
3	ESPI_CS#	SMB_CLK_MAIN	4
5	ESPI_RST#	SMB_DATA_MAIN	6
7	ESPI_IO3	ESPI_IO2	8
9	+3V	ESPI_IO1	10
11	ESPI_IO0	GND	12
13		S_PWRDWN#	14
15	+3VSB	DUMMY	16
17	GND	GND	18



6 : M.2 Key-M Socket (M2_M1)

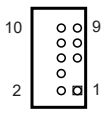
Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	NA	NA	6
7	NA	NA	8
9	GND	LED	10
11	NA	+3.3V	12
13	NA	+3.3V	14
15	GND	+3.3V	16
17	NA	+3.3V	18
19	NA	NA	20
21	GND	NA	22
23	NA	NA	24
25	NA	NA	26
27	GND	NA	28
29	NA	NA	30
31	NA	NA	32
33	GND	NA	34
35	NA	NA	36
37	NA	NA	38
39	GND	SMB_CLK	40
41	PERn0	SMB_DATA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETP0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

7 : M.2 Key-E Socket (M2_E1)

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	USB_D+	+3.3V	4
5	USB_D-	NA	6
7	GND	NA	8
9	CNV_WGR_D1-	CNV_RF_RESET	10
11	CNV_WGR_D1+	NA	12
13	GND	MODEM_CLKREQ	14
15	CNV_WGR_D0-	NA	16
17	CNV_WGR_D0+	GND	18
19	GND	NA	20
21	CNV_WGR_CLK-	CNV_BRI_RSP	22
23	CNV_WGR_CLK+		
		CNV_BGI_DT	32
33	GND	CNV_RGI_RSP	34
35	PETp	CNV_BRI_DT	36
37	PETn	NA	38
39	GND	NA	40
41	PERp	NA	42
43	PERn	NA	44
45	GND	NA	46
47	PEFCLKp	NA	48
49	PEFCLKn	SUSCLK	50
51	GND	PERST0#	52
53	CLKREQ#	W_DISABLE1#	54
55	NA	W_DISABLE2#	56
57	GND	SMB_DATA	58
59	CNV_WT_D1-	SMB_CLK	60
61	CNV_WT_D1+	NA	62
63	GND	NA	64
65	CNV_WT_D0-	NA	66
67	CNV_WT_D0+	NA	68
69	GND	NA	70
71	CNV_WT_CLK-	+3.3V	72
73	CNV_WT_CLK+	+3.3V	74
75	GND		

10 : COM_CC_TTL_SEL1

Pin	Signal Name	Signal Name	Pin
1	+5V	GND	2
3	NA	NA	4
5	TTXD_TTL5V	RRXD_TTL5V	6
7	TTXD	RRXD	8
9	TTXD_RS232	RRXD_RS232	10



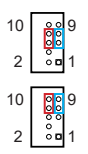
COM_CC_TTL_SEL1:79 MINI_JUMPER

COM_CC_TTL_SEL1:80 MINI_JUMPER

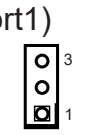
Open: CCTALK function

• Supported by CCTALK Card (optional)
https://www.asrockind.com/UART-CCTALK

5-7 + 6-8 : TTL function
7-9 + 8-10 : COM (RS232) (Default)

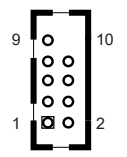


COM Port Pin9 PWR Setting Jumpers
11 : PWR_COM4 (For COM Port4)
PWR_COM3 (For COM Port3)
13 : PWR_COM2 (For COM Port2)
PWR_COM1 (For COM Port1)
Open : +0V
1-2 : +5V (Default)
2-3 : +12V



12 : Internal COM Port Headers (COM1) (RS232/422/485)* (COM2~4) (RS232)

Pin	Signal Name	Signal Name	Pin
1	DDCD#	RRXD	2
3	TTXD	DDTR#	4
5	GND	DDSR#	6
7	RRTS#	CCTS#	8
9	PWR		10



* This motherboard supports RS232/422/485 on COM1 port. Please refer to the table below for the pin definition. In addition, COM1 port (RS232/422/485) can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

COM1 Port Pin Definition

Pin	RS232	RS422	RS485
1	DCD	TX-	RTX-
2	RXD	TX+	RTX+
3	TXD	RX+	NA
4	DTR	RX-	NA
5	GND	GND	GND
6	DSR	NA	NA
7	RTS	NA	NA
8	CTS	NA	NA
9	PWR	PWR	PWR
10	NA	NA	NA

COM2~4 Port Pin Definition

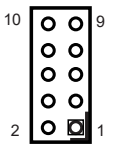
Pin	RS232
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	PWR
10	NA

14 : Digital Input/Output Default Value Setting (JGPIO_SET1)

1-2: Pull-High (Default)
2-3: Pull-Low

15 : Digital Input/Output Pin Header (JGPIO1)

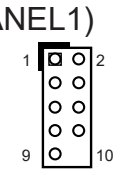
Pin	Signal Name	Signal Name	Pin
1	GPP_B18	GPP_B22	2
3	GPP_B19	GPP_B23	4
5	GPP_H06	GPP_E05	6
7	GPP_H07	GPP_E07	8
9	+3V	GND	10



Parameter	Range
GPIO input Low Voltage	Max. 0.83V
GPIO input High Voltage	Min. 2.48V
GPIO output Low Voltage	Max. 0.45V
GPIO output High Voltage	Min. 2.85V
Note: Max. load per GPIO pin: 3mA JGPIO1 Pin 9 - JGPIOPWR_R, Current Max. 1A	

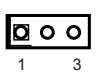
16 : System Panel Header (PANEL1)

Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	+5VSB		10

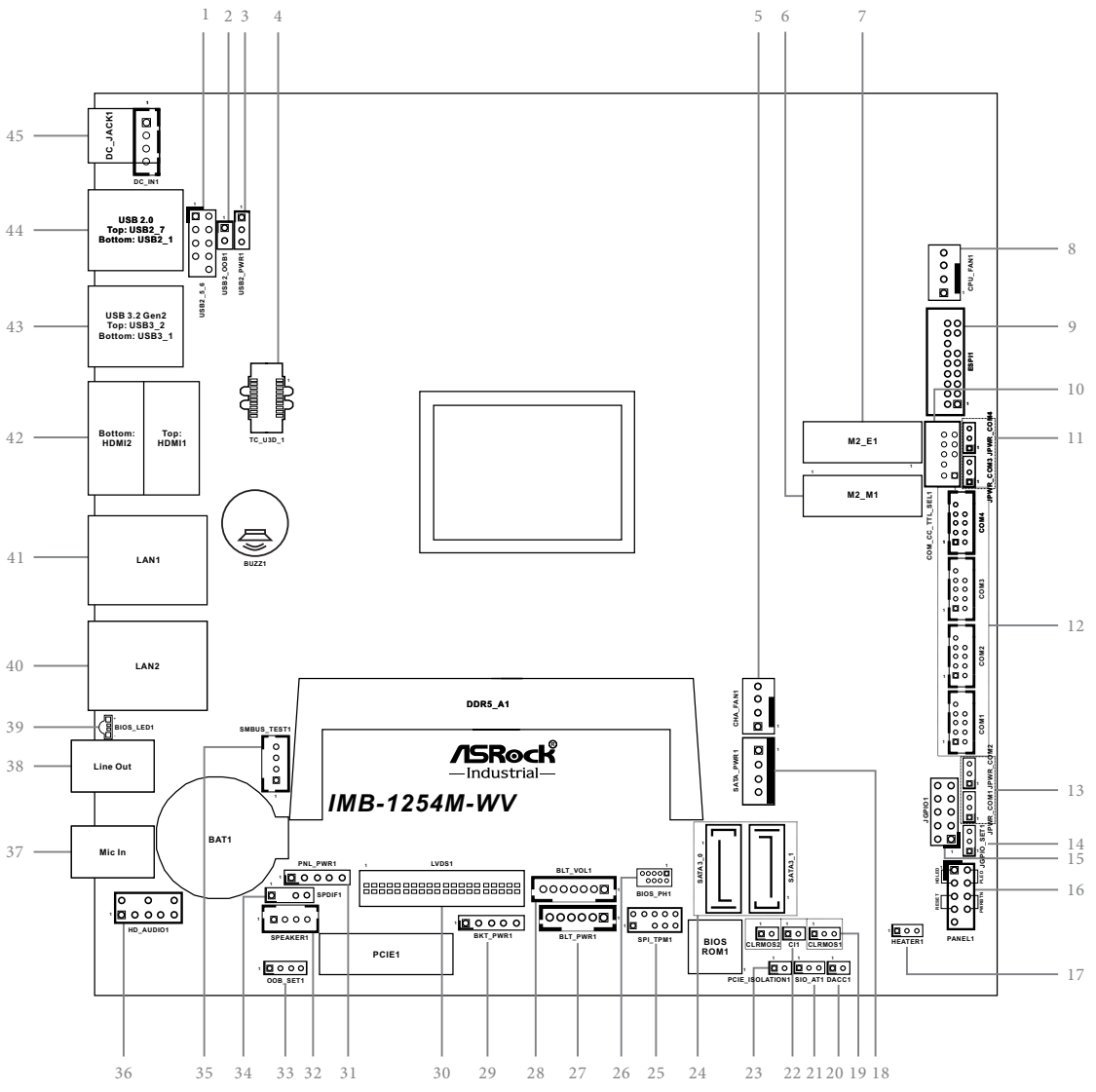


17 : Heater Header (HEATER1)

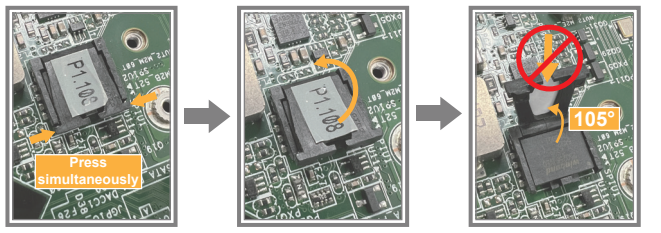
Pin	Signal Name
1	Heater_PWR (5V/1A)
2	GND
3	NTC (Negative Temperature Coefficient) thermistors

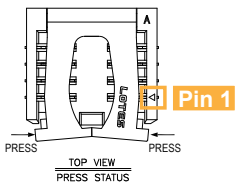


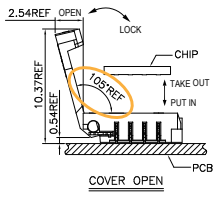
• The 10k Ohm NTC thermistors is suggested.
• Deep mode is not supported when the preheat function is enabled.



Installation of LOTES ROM Socket







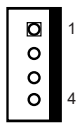
- Do not press one side of the actuator cover at a time. Always apply even and simultaneous force to both sides to avoid damage.
- Do not apply force to the actuator cover after the IC is inserted, especially when it is fully opened at 105 degrees. Pressing vertically at this angle may cause the cover to break.

- The white dot (Pin 1) on the ROM must align with the Pin 1 position of the socket (white arrow area).
- Ensure the white dot on the ROM is facing outward from the socket.

Warning: Incorrect installation may damage the chipset and motherboard. Refer to the picture for proper orientation.

18 : SATA Power Output Connector (SATA_PWR1)

Pin	Signal Name
1	+5V
2	GND
3	GND
4	+12V



19 : Clear CMOS Jumpers

CLRMOS1
1-2: Normal (Default)
2-3: Clear CMOS

CLRMOS2
Open: Normal (Default)
Short: Auto Clear CMOS When AC Power On

20 : DACC Jumper (DACC1)

Open: Normal
Short: Auto Clear CMOS (Default)

• Note: Auto clear CMOS when system boot improperly.

21 : ATX/AT Mode Jumper (SIO_AT1)

1-2 : AT Mode
2-3 : ATX Mode (Default)

22 : Chassis Intrusion Header (CI1)

Open: Normal (Default)
Short: Active Case Open

23 : PCIE_ISOLATION1

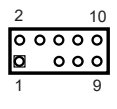
Pin	Signal Name
1	PSON#
2	GND

24 : SATA3 Connectors (SATA3_0, SATA3_1)

Pin	Signal Name
1	GND
2	SATA-A+
3	SATA-A-
4	GND
5	SATA-B-
6	SATA-B+
7	GND

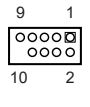
25 : SPI_TPM Header (SPI_TPM1)

Pin	Signal Name	Signal Name	Pin
1	TPM PWR	RST#	2
3		CS#	4
5	IRA	MOSI	6
7	MISO	GND	8
9	CLK	GND	10



26 : BIOS_PH1 (Programming Header)

*For offline BIOS flashing with the EQUIP-USB3-SPI programmer only.

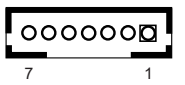


27 : Backlight Power Connector (BLT_PWR1)

Pin	Signal Name
1	GND
2	GND
3	CON_LBKLT_CTL
4	CON_LBKLT_EN
5	LCD_BLT_VCC
6	LCD_BLT_VCC

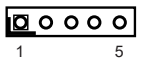
28 : Backlight Volume Control (BLT_VOL1)

Pin	Signal Name
1	NA
2	NA
3	PWRDN
4	BLT_UP
5	BLT_DW
6	GND
7	GND



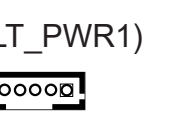
29 : eDP and LVDS Backlight Power Select (LCD_BLT_VCC) (BKT_PWR1)

1-2: LCD_BLT_VCC: +5V (Default)
2-3: LCD_BLT_VCC: +12V
4-5: LCD_BLT_VCC: DC_IN



30 : LVDS Panel Connector (LVDS1)*

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	+3.3V	N/A	4
5	N/A	LVDS_A_DATA0#	6
7	LVDS_A_DATA0	PD (Panel Detection)	8
9	LVDS_A_DATA1#	LVDS_A_DATA1	10
11	GND	LVDS_A_DATA2#	12
13	LVDS_A_DATA2	GND	14
15	LVDS_A_DATA3#	LVDS_A_DATA3	16
17	GND	LVDS_A_CLK#	18
19	LVDS_A_CLK	GND	20
21	LVDS_B_DATA0#	LVDS_B_DATA0	22
23	GND	LVDS_B_DATA1#	24
25	LVDS_B_DATA1	GND	26
27	LVDS_B_DATA2#	LVDS_B_DATA2	28
29	DPLVDD_EN	LVDS_B_DATA3#	30
31	LVDS_B_DATA3	GND	32
33	LVDS_B_CLK#	LVDS_B_CLK	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40



* PD (Panel Detection): Connect this pin to LVDS Panel's Ground pin to detect Panel detection.

31 : eDP and LVDS Panel Power Select (LCD_VCC) (PNL_PWR1)

1-2: LCD_VCC: +3V (Default)
2-3: LCD_VCC: +5V
4-5: LCD_VCC: +12V

32 : 3W Audio AMP Output Wafer (SPEAKER1)

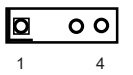
Pin	Signal Name
1	OUTLN
2	OUTLP
3	OUTRP
4	OUTRN

33 : OOB_SET1 (Onboard OOB only)

1-2: Boot Source From SPI Mode (Default)
2-3: Boot Source From USB Mode
3-4: Factory Reset

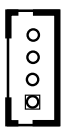
34 : SPDIF Header (SPDIF1)

Pin	Signal Name
1	+5V
2	
3	SPDIF OUT
4	GND



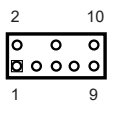
35 : SMBUS_TEST1

Pin	Signal Name
1	GPP_E16
2	SMB_CLK_MAIN
3	SMB_DATA_MAIN
4	GND



36 : Front Panel Audio Header (HD_AUDIO1)

Pin	Signal Name	Signal Name	Pin
1	LIN1_L	GND	2
3	LIN1_R		4
5	HPOUT_R	LIN1_JD	6
7	GND		8
9	HPOUT_L	J_SENSE	10

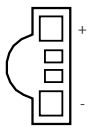


37 : Audio Jack: Pink - Mic In

38 : Audio Jack: Green - Line Out

39 : BIOS_LED1 (Onboard OOB only)

Status	Description
Blue	BIOS Backup
Red	BIOS Recovery



40 : RJ-45 LAN Port (LAN2)

41 : RJ-45 LAN Port (LAN1)

42 : Top : HDMI Port (HDMI1)
Bottom : HDMI Port (HDMI2)

43 : Top : USB 3.2 Gen2 Port (USB3_2)
Bottom : USB 3.2 Gen2 Port (USB3_1)

44 : Top : USB 2.0 Port (USB2_7)
Bottom : USB 2.0 Port (USB2_1)

45 : DC-In Jack (DC_JACK1)

4-pin DC-in Wafer (DC_IN1) (BOM option)

Pin	Signal Name
1	GND
2	DC Input
3	DC Input
4	GND