



P/N: 15G06M08900AK V1.0

Jumpers and Headers Setting Guide

ASRock

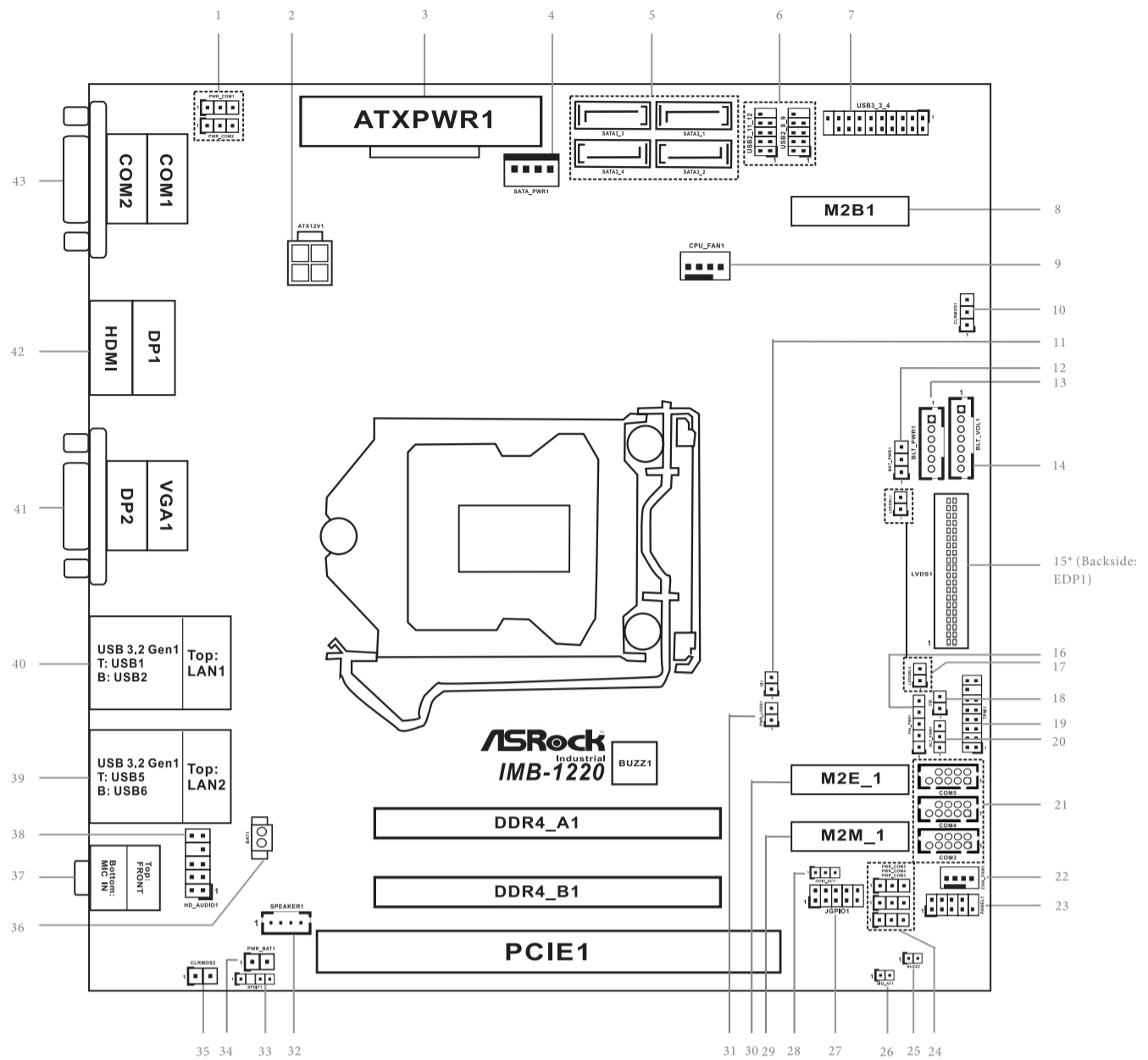
— Industrial —

IMB-1220

IMB-1221

IMB-X1220

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COM Port PWR Setting Jumpers

- 1 : PWR_COM1 (For COM Port1)
- PWR_COM2 (For COM Port2)
- 24 : PWR_COM3 (For COM Port3)
- PWR_COM4 (For COM Port4)
- PWR_COM5 (For COM Port5) (For IMB-1220 / IMB-X1220 only)

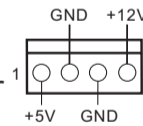
1-2 : +5V
2-3 : +12V

2 : 4-pin ATX Power Input/Output Connector

3 : 24-pin ATX Power Input Connector

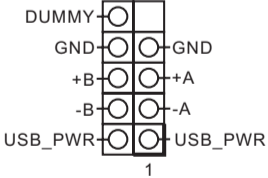


4 : SATA Power Output Connector

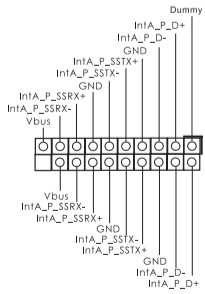


5 : SATA3 Connectors (SATA3_1~4)

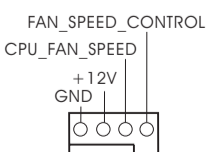
6 : USB2.0 Headers (USB2_8_9, USB2_11_12)
(USB2_11_12 is for IMB-1220 / IMB-X1220 only)



7 : USB3.2 Gen1 Header (USB3_3_4)

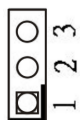


9 : 4-Pin CPU FAN Connector (+12V) (CPU_FAN1)



10 : Clear CMOS Header (CLRMOS1)

1-2 : Normal
2-3 : Clear CMOS



Chassis Intrusion Headers (CI1, CI2)

- 11 : CI1 :
Close : Active Case Open
Open : Normal
- 18 : CI2 :
Close : Normal
Open : Active Case Open



12 : Backlight Power Select (LCD_BLT_VCC) (BKT_PWR1)
1-2 : LCD_BLT_VCC : +5V
2-3 : LCD_BLT_VCC : +12V



13 : Inverter Power Control Wafer (BLT_PWR1)



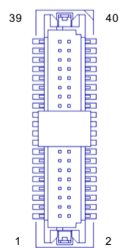
PIN	Signal Name
1	GND
2	GND
3	CON_LBKLT_CTL
4	CON_LBKLT_EN
5	LCD_BLT_VCC
6	LCD_BLT_VCC

14 : Backlight Volume Control (BLT_VOL1)



PIN	Signal Name
1	GPIO_VOL_UP
2	GPIO_VOL_DW
3	PWRDN
4	BLT_UP
5	BLT_DW
6	GND
7	GND

15* : LVDS Panel Connector



PIN	Signal Name	PIN	Signal Name
39	LCD_BLT_VCC	40	LCD_BLT_VCC
37	CON_LBKLT_CTL	38	LCD_BLT_VCC
35	GND	36	CON_LBKLT_EN
33	LVDS_B_CLK#	34	LVDS_B_CLK
31	LVDS_B_DATA3	32	GND
29	DPLVDD_EN	30	LVDS_B_DATA3#
27	LVDS_B_DATA2#	28	LVDS_B_DATA2
25	LVDS_B_DATA1	26	GND
23	GND	24	LVDS_B_DATA1#
21	LVDS_B_DATA0#	22	LVDS_B_DATA0
19	LVDS_A_CLK	20	GND
17	GND	18	LVDS_A_CLK#
15	LVDS_A_DATA3#	16	LVDS_A_DATA3
13	LVDS_A_DATA2	14	GND
11	GND	12	LVDS_A_DATA2#
9	LVDS_A_DATA1#	10	LVDS_A_DATA1
7	LVDS_A_DATA0	8	PD (Panel Detection)
5	LDDC_DATA	6	LVDS_A_DATA0#
3	+3.3V	4	LDDC_CLK
1	LCD_VCC	2	LCD_VCC

* PD (Panel Detection): Connect this pin to LVDS Panel's Ground pin to detect Panel detection.

*** eDP Connector (on the Backside of PCB)**



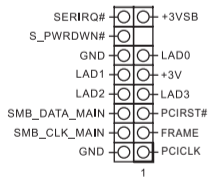
16 : Panel Power Select (LCD_VCC) (PNL_PWR1)
1-2 : LCD_VCC : +3V
2-3 : LCD_VCC : +5V
4-5 : LCD_VCC : +12V



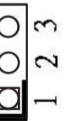
17 : LVDSBL1 :
Open : Protect LCD_VCC
Short : No Protect LCD_VCC
LVDSBL2 :
Open : Protect LCD_BLT_VCC
Short : No Protect LCD_BLT_VCC



19 : TPM Header (For IMB-1220 / IMB-X1220 only)



20 : Backlight Control Level (CON_LBKLT_CTL) (BLT_PWM1)
1-2 : From eDP PWM to CON_LBKLT_CTL
2-3 : From LVDS PWM to CON_LBKLT_CTL

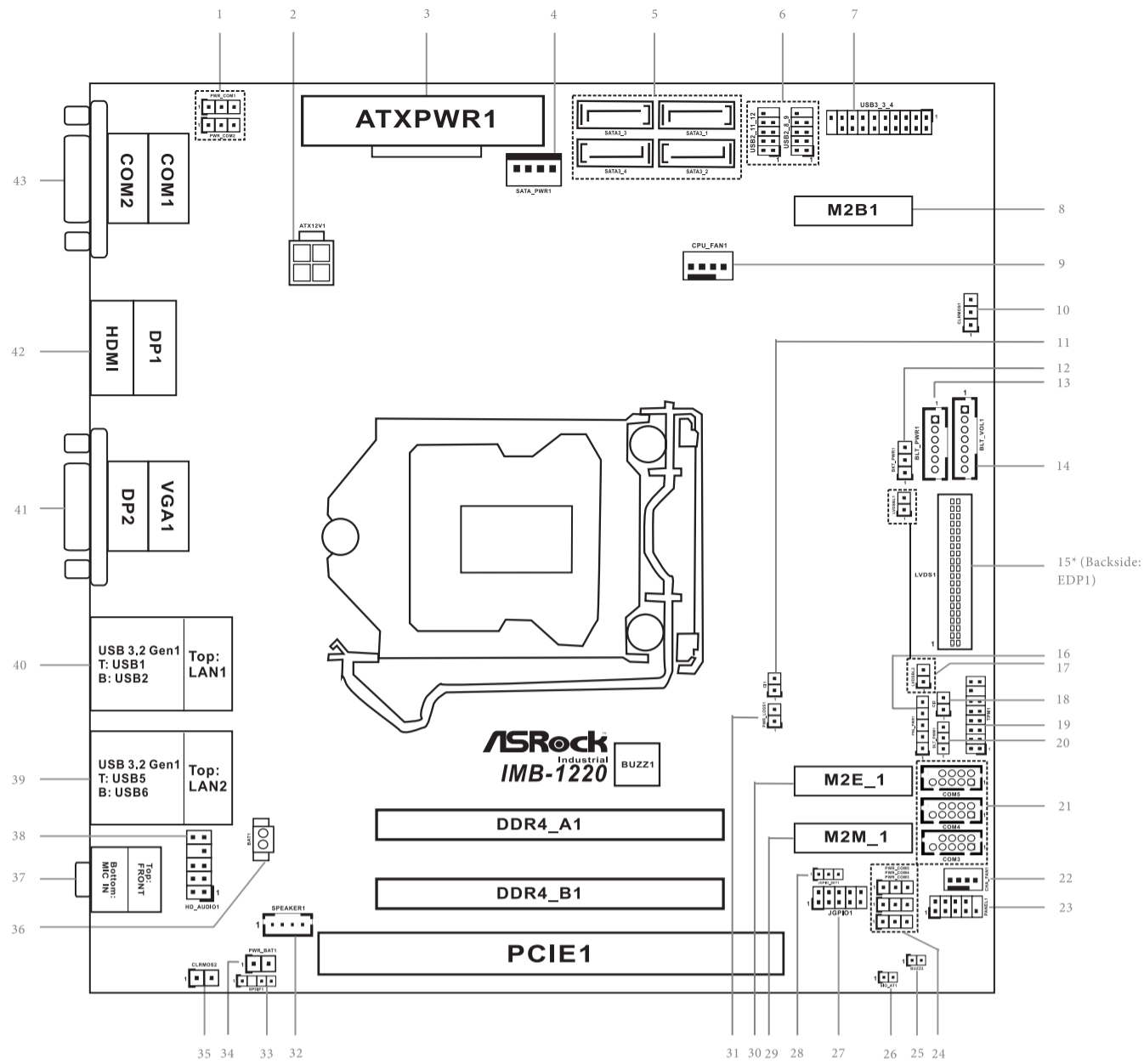


21 : COM Port Headers (COM3, 4, 5) (RS232)
(COM5 is for IMB-1220 / IMB-X1220 only)

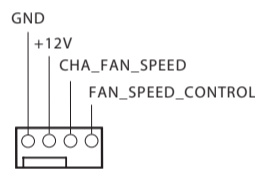


PIN	Signal Name	PIN	Signal Name	PIN	Signal Name	PIN	Signal Name	PIN	Signal Name
10	N/A	8	CCTS#	6	DDSR#	4	DDTR#	2	RRXD#
9	PWR	7	RRTS#	5	GND	3	TTXD	1	DDCD#

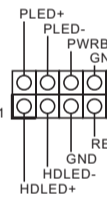
40	NA
39	LCD_BLT_VCC
38	LCD_BLT_VCC
37	LCD_BLT_VCC
36	LCD_BLT_VCC
35	NA
34	NA
33	CON_LBKLT_CTL
32	CON_LBKLT_EN
31	GND
30	GND
29	GND
28	GND
27	eDP_HPDI_CON
26	GND
25	GND
24	GND
23	GND
22	NA
21	LCD_VCC
20	LCD_VCC
19	LCD_VCC
18	LCD_VCC
17	GND
16	eDP_AUX#_CON
15	eDP_AUX#_CON
14	GND
13	eDP_TX#_CON
12	eDP_TX#_CON
11	GND
10	eDP_TX1_CON
9	eDP_TX#1_CON
8	GND
7	eDP_TX2_CON
6	eDP_TX#2_CON
5	GND
4	eDP_TX3_CON
3	eDP_TX#3_CON
2	GND
1	NA
PIN	Signal Name



22 : 4-Pin Chassis FAN Connector (+12V)



23 : System Panel Header



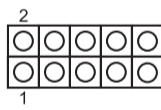
25 : Buzzer



26 : SIO_AT1
Open : ATX Mode
Short : AT Mode

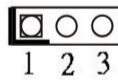


27 : Digital Input/Output Pin Header (JGPIO1)



PIN	Signal Name	PIN	Signal Name	PIN	Signal Name	PIN	Signal Name	PIN	Signal Name
2	SIO_GP71	4	SIO_GP72	6	SIO_GP73	8	SIO_GP74	10	GND
1	SIO_GP75	3	SIO_GP76	5	SIO_GP77	7	SIO_GP80	9	JGPIO_PWR

28 : Digital Input / Output Default Value Setting (JGPIO_SET1)
1-2 : Pull-High
2-3 : Pull-Low



31 : PWR LOSS Header (PWR_LOSS1)
Short : Power Loss
Open : no Power Loss

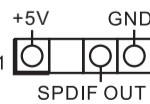


32 : 3W Audio AMP Output Wafer



PIN	Signal Name	PIN	Signal Name	PIN	Signal Name	PIN	Signal Name
1	OUTLN	2	OUTLP	3	OUTRP	4	OUTRN

33 : SPDIF Header



34 : PWR_BAT1
Open : Normal
Short : Charge Battery



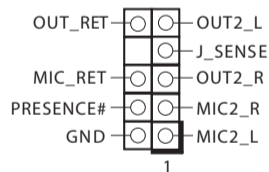
35 : Clear CMOS Header (CLRMOS2)
Open : Normal
Short : Auto Clear CMOS (Power Off)



36 : Battery Connector

37 : Audio Output
Green - Line Out
Pink - Mic In

38 : Front Panel Audio Header



39 : Top : RJ45 LAN Port (LAN2)
Bottom :
USB3.2 Gen1 Ports (USB_5_6) (IMB-1220 / IMB-X1220)
USB2.0 Ports (USB_5_6) (IMB-1221)
40 : Top : RJ45 LAN Port (LAN1)
Bottom : USB3.2 Gen1 Ports (USB_1_2)
41 : Top : D-Sub Port (VGA1)
Bottom : DisplayPort (DP2)
42 : Top : DisplayPort (DP1)
Bottom : HDMI Port (HDMI)
43 : Top : COM Port (COM1) (RS232/422/485)*
Bottom : COM Port (COM2) (RS232/422/485)*

* Please refer to below table for the pin definition. In addition, they can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

COM1, 2 Port Pin Definition

PIN	RS232	RS422	RS485
1	DCD	TX-	RTX-
2	RXD	RX+	N/A
3	TXD	TX+	RTX+
4	DTR	RX-	N/A
5	GND	GND	GND
6	DSR	N/A	N/A
7	RTS	N/A	N/A
8	CTS	N/A	N/A
9	+5V / +12V	N/A	N/A

Back Side :
SIM Card Socket (SIM1)
eDP Connector (EDP1, refer to No. 15)
MCU Connector (MCU_CON1)

M.2 Socket Pin Definition

8 : M.2 Key-B Socket (M2B1)

Pin	Signal	Signal	Pin
1	NA	+3.3V	2
3	GND	+3.3V	4
5	GND	Full Card Power off	6
7	USB D+	W_DISABLE	8
9	USB D-	WLAN_LED#	10
11	GND		12
13	NA	NA	14
15	NA	NA	16
17	GND	NA	18
19	USB3_RX+	UIM_RESET	20
21	USB3_RX-	UIM_CLK	22
23	GND	UIM_PWR	24
25	USB3_TX+	UIM_DATA	26
27	USB3_TX-	UIM_PWR	28
29	GND	NA	30
31	PETn0	NA	32
33	PETp0	NA	34
35	GND	NA	36
37	PETn1	NA	38
39	PETp1	NA	40
41	GND	NA	42
43	PEFCLKp	CLKREQ#	44
45	PEFCLKn	WAKE#	46
47	GND	NA	48
49	NA	NA	50
51	NA	NA	52
53	NA	NA	54
55	NA	NA	56
57	NA	NA	58
59	NA	NA	60
61	NA	NA	62
63	NA	NA	64
65	NA	NA	66
67	NA	NA	68
69	NA	NA	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	NA	+3.3V	76

29 : M.2 Key-M Socket (M2M_1)

* For IMB-1221, if M2M_1 is occupied by a SATA-type M.2 device, SATA3_1 will be disabled.

Pin	Signal	Signal	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	PERn3	NA	6
7	PERp3	NA	8
9	GND	SATA_LED	10
11	PETn0	+3.3V	12
13	PETp0	+3.3V	14
15	GND	+3.3V	16
17	PERn2	+3.3V	18
19	PERp2	NA	20
21	GND	NA	22
23	PETn2	NA	24
25	PETp2	NA	26
27	GND	NA	28
29	PERn1	NA	30
31	PERp1	NA	32
33	GND	NA	34
35	PETn1	NA	36
37	PETp1	DEVSLP	38
39	GND	SMB_CLK	40
41	PERn0/SATA-B+	SMB_DATA	42
43	PERp0/SATA-B-	NA	44
45	GND	NA	46
47	PETn0/SATA-B-	NA	48
49	PETp0/SATA-B+	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	WAKE#	54
55	PEFCLKp	NA	56
57	GND	NA	58
59	NA	NA	60
61	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		76

30 : M.2 Key-E Socket (M2E_1)

Pin	Signal	Signal	Pin
1	GND	+3.3V	2
3	USB D+	+3.3V	4
5	USB D-	NA	6
7	GND	NA	8
9	CNV_WSR_D0	CNV_SF_RESET	10
11	CNV_WSR_D1+	NA	12
13	GND	MODEM_CLKREQ	14
15	CNV_WSR_D0-	NA	16
17	CNV_WSR_D0+	GND	18
19	GND	NA	20
21	CNV_WSR_CLK-	CNV_BBI_RSP	22
23	CNV_WSR_CLK+		24
25	GND	NA	26
27	PETp	CNV_BBI_DT	28
29	PETn	CNV_BBI_DT	30
31	GND	NA	32
33	PEFCLKp	NA	34
35	PEFCLKn	NA	36
37	GND	NA	38
39	GND	NA	40
41	PERn	NA	42
43	GND	NA	44
45	PEFCLKp	NA	46
47	PEFCLKn	NA	48
49	GND	NA	50
51	GND	SUSCLK	52
53	CLKREQ#	PERST#	54
55	WAKE#	W_DISABLE#	56
57	GND	W_DISABLE#	58
59	CNV_WT_D1-	SMB_DATA	60
61	CNV_WT_D1+	SMB_CLK	62
63	GND	NA	64
65	CNV_WT_DD-	CLKIN_XTAL_LCP	66
67	CNV_WT_DD+	NA	68
69	GND	NA	70
71	CNV_WT_CLK-	NA	72
73	CNV_WT_CLK+	+3.3V	74
75	GND	+3.3V	76