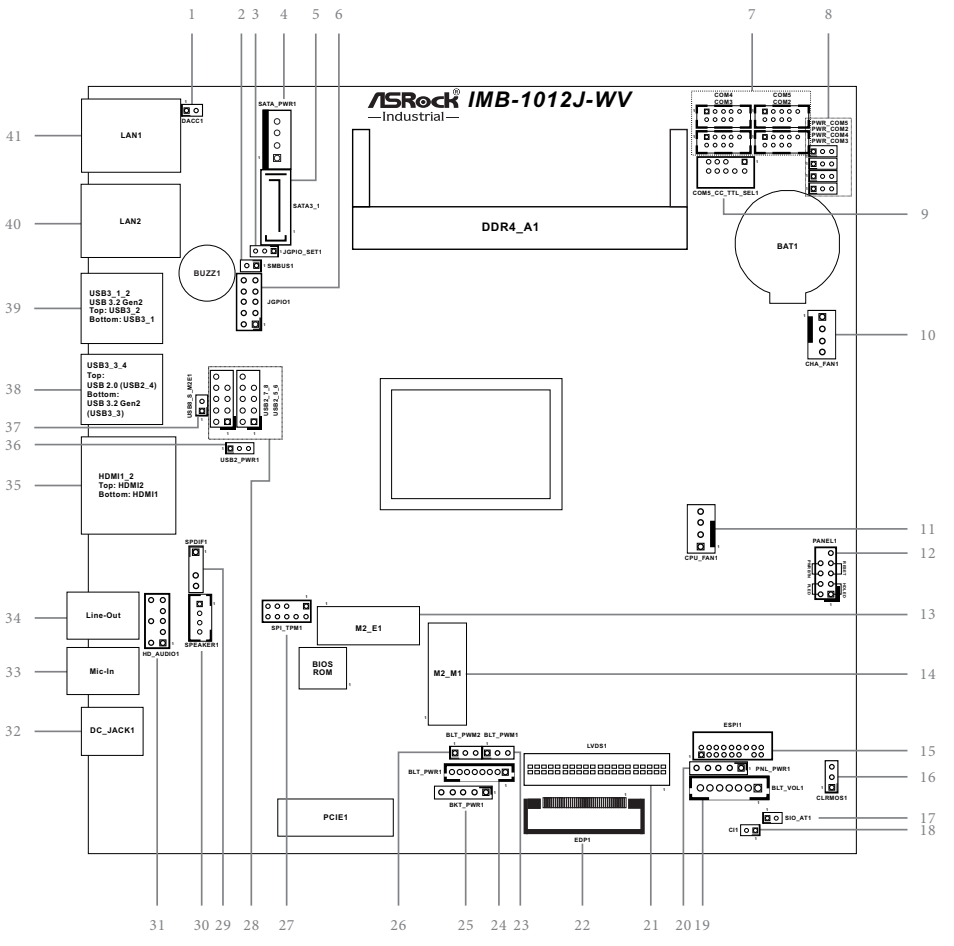
Jumpers and Headers Setting Guide

ASRock Industrial

IMB-1012J-WV

Revision History

Date	Description
May 29, 2025	First Release
June 18, 2025	Second Release
July 11, 2025	Third Release



1 : DACC Jumper (DACC1)

Open: Normal
Short: Auto Clear CMOS (Default)

• Note: Auto clear CMOS when system boot improperly.

2 : SMBUS1

Pin	Signal Name
1	SMB_DATA
2	SMB_CLK

3 : Digital Input/Output Default Value Setting (JGPIO_SET1)

1-2: Pull-High (Default)
2-3: Pull-Low

4 : SATA Power Output Connector (SATA_PWR1)

Pin	Signal Name
1	+5V
2	GND
3	GND
4	+12V

5 : SATA3 Connector (SATA3_1)

Pin	Signal Name
1	GND
2	SATA-A+
3	SATA-A-
4	GND
5	SATA-B-
6	SATA-B+
7	GND

6 : Digital Input/Output Pin Header (JGPIO1)

Pin	Signal Name	Signal Name	Pin
1	GPP_A14	GPP_B15	2
3	GPP_A15	GPP_E1	4
5	GPP_A16	GPP_E2	6
7	GPP_A17	GPP_E13	8
9	+3V	GND	10

Parameter	Range
GPIO input Low Voltage	Max. 0.83V
GPIO input High Voltage	Min. 2.48V
GPIO output Low Voltage	Max. 0.45V
GPIO output High Voltage	Min. 2.85V
Note: Max. load per GPIO pin: 3mA JGPIO1 Pin 9 - JGPIOPWR_R, Current Max. 1A	

7 : Internal COM Port Headers (COM2) (RS232/422/485)* (COM3~5) (RS232)

Pin	Signal Name	Signal Name	Pin
1	DDCD#	RRXD	2
3	TTXD	DDTR#	4
5	GND	DDSR#	6
7	RRTS#	CCTS#	8
9	PWR		10

* This motherboard supports RS232/422/485 on COM2 port. Please refer to the table below for the pin definition. In addition, COM2 port (RS232/422/485) can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

COM2 Port Pin Definition

Pin	RS232	RS422	RS485
1	DCD	TX-	RTX-
2	RXD	TX+	RTX+
3	TXD	RX+	NA
4	DTR	RX-	NA
5	GND	GND	GND
6	DSR	NA	NA
7	RTS	NA	NA
8	CTS	NA	NA
9	PWR	PWR	PWR
10	NA	NA	NA

COM3~5 Port Pin Definition

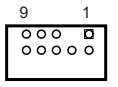
Pin	RS232
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	PWR
10	NA

8 : COM Port Pin9 PWR Setting Jumpers

PWR_COM2 (For COM Port2)
PWR_COM3 (For COM Port3)
PWR_COM4 (For COM Port4)
PWR_COM5 (For COM Port5)
Open : +0V
1-2 : +5V (Default)
2-3 : +12V

9 : COM5_CC_TTL_SEL1

Pin	Signal Name	Signal Name	Pin
1	GND	+5V	2
3	NA	NA	4
5	RRXD_TTL5V	TTXD_TTL5V	6
7	NA	NA	8
9	NA	NA	10



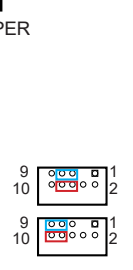
COM_CC_TTL_SEL1:79 MINI_JUMPER

COM_CC_TTL_SEL1:80 MINI_JUMPER

Open: CCTALK function

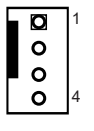
• Supported by CCTALK Card (optional)
https://www.asrockind.com/UART-CCTALK

5-7 + 6-8 : TTL function
7-9 + 8-10 : COM (RS232) (Default)



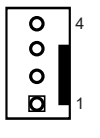
10 : Chassis FAN Connector (+12V) (CHA_FAN1)

Pin	Signal Name
1	GND
2	+12V
3	CHA_FAN_SPEED
4	FAN_SPEED_CONTROL



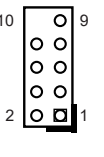
11 : CPU FAN Connector (+12V) (CPU_FAN1)

Pin	Signal Name
1	GND
2	+12V
3	CPU_FAN_SPEED
4	FAN_SPEED_CONTROL



12 : System Panel Header (PANEL1)

Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	GND		10



13 : M.2 Key-E Socket (M2_E1)

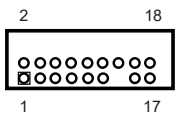
Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	USB_D+	+3.3V	4
5	USB_D-	NA	6
7	GND	NA	8
9	CNV_WGR_D1-	CNV_RF_RESET	10
11	CNV_WGR_D1+	NA	12
13	GND	MODEM_ CLKREQ	14
15	CNV_WGR_D0-	NA	16
17	CNV_WGR_D0+	GND	18
19	GND	NA	20
21	CNV_WGR_CLK-	CNV_BRI_RSP	22
23	CNV_WGR_ CLK+		
		CNV_BGI_DT	32
33	GND	CNV_RGI_RSP	34
35	PETp	CNV_BRI_DT	36
37	PETn	NA	38
39	GND	NA	40
41	PERp	NA	42
43	PERn	NA	44
45	GND	NA	46
47	PEFCLKp	NA	48
49	PEFCLKn	SUSCLK	50
51	GND	PERST0#	52
53	CLKREQ#	W_DISABLE1#	54
55	NA	W_DISABLE2#	56
57	GND	SMB_DATA	58
59	CNV_WT_D1-	SMB_CLK	60
61	CNV_WT_D1+	NA	62
63	GND	NA	64
65	CNV_WT_D0-	NA	66
67	CNV_WT_D0+	NA	68
69	GND	NA	70
71	CNV_WT_CLK-	+3.3V	72
73	CNV_WT_CLK+	+3.3V	74
75	GND		

14 : M.2 Key-M Socket (M2_M1)

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	NA	NA	6
7	NA	NA	8
9	GND	LED	10
11	NA	+3.3V	12
13	NA	+3.3V	14
15	GND	+3.3V	16
17	NA	+3.3V	18
19	NA	NA	20
21	GND	NA	22
23	NA	NA	24
25	NA	NA	26
27	GND	NA	28
29	NA	NA	30
31	NA	NA	32
33	GND	NA	34
35	NA	NA	36
37	NA	DEVSLP	38
39	GND	NA	40
41	PERn0	NA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETP0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

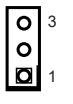
15 : ESPI Header (ESPI1)

Pin	Signal Name	SiSignal Name	Pin
1	ESPI_CLK	GND	2
3	ESPI_CS#	SMB_CLK_MAIN	4
5	ESPI_RST#	SMB_DATA_ MAIN	6
7	ESPI_IO3	ESPI_IO2	8
9	+3V	ESPI_IO1	10
11	ESPI_IO0	GND	12
13		S_PWRDWN#	14
15	+3VSB	DUMMY	16
17	GND	GND	18



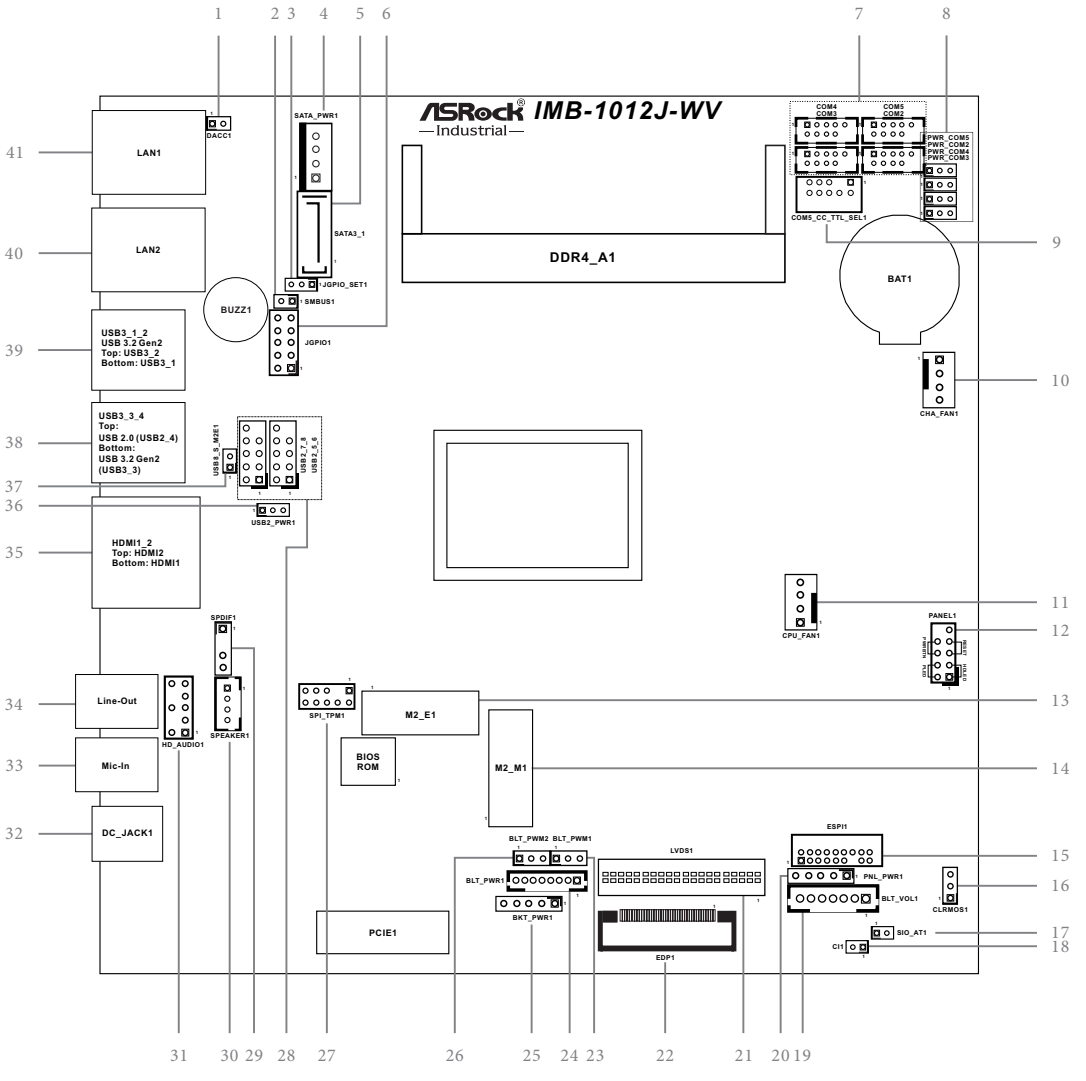
16 : Clear CMOS Jumper (CLRMOS1)

1-2: Normal (Default)
2-3: Clear CMOS



17 : ATX/AT Mode Jumper (SIO_AT1)

Short: ATX Mode (Default)
Open: AT Mode

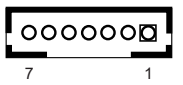


18 : Chassis Intrusion Header (CI1)

Open: Normal (Default)
Short: Active Case Open

19 : Backlight Volume Control (BLT_VOL1)

Pin	Signal Name
1	GPIO_VOL_UP
2	GPIO_VOL_DW
3	PWRDN
4	BLT_UP
5	BLT_DW
6	GND
7	GND

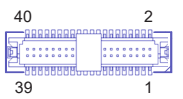


20 : eDP and LVDS Panel Power Select (LCD_VCC) (PNL_PWR1)

1-2: LCD_VCC: +3V (Default)
2-3: LCD_VCC: +5V
4-5: LCD_VCC: +12V

21 : LVDS Panel Connector (LVDS1)**

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	+3.3V	N/A	4
5	N/A	LVDS_A_DATA0#	6
7	LVDS_A_DATA0	PD (Panel Detection)	8
9	LVDS_A_DATA1#	LVDS_A_DATA1	10
11	GND	LVDS_A_DATA2#	12
13	LVDS_A_DATA2	GND	14
15	LVDS_A_DATA3#	LVDS_A_DATA3	16
17	GND	LVDS_A_CLK#	18
19	LVDS_A_CLK	GND	20
21	LVDS_B_DATA0#	LVDS_B_DATA0	22
23	GND	LVDS_B_DATA1#	24
25	LVDS_B_DATA1	GND	26
27	LVDS_B_DATA2#	LVDS_B_DATA2	28
29	DPLVDD_EN	LVDS_B_DATA3#	30
31	LVDS_B_DATA3	GND	32
33	LVDS_B_CLK#	LVDS_B_CLK	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40



** PD (Panel Detection): Connect this pin to LVDS Panel's Ground pin to detect Panel detection.

22 : eDP Connector (EDP1)**

Pin	Signal Name
1	NA
2	GND
3	eDP_TX#3_CON
4	eDP_TX3_CON
5	GND
6	eDP_TX#2_CON
7	eDP_TX2_CON
8	GND
9	eDP_TX#1_CON
10	eDP_TX1_CON
11	GND
12	eDP_TX#0_CON
13	eDP_TX0_CON
14	GND
15	eDP_AUX_CON
16	eDP_AUX#_CON
17	GND
18	LCD_VCC
19	LCD_VCC
20	LCD_VCC
21	LCD_VCC
22	NA
23	GND
24	GND
25	GND
26	GND
27	eDP_HPD_CON
28	GND
29	GND
30	GND
31	GND
32	eDP_BKLTEN
33	eDP_BKLTCTL_R
34	SMB_DATA_MAIN
35	SMB_CLK_MAIN
36	LCD_BLT_VCC
37	LCD_BLT_VCC
38	LCD_BLT_VCC
39	LCD_BLT_VCC
40	NA

24 : Backlight Power Connector (BLT_PWR1)

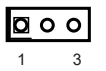
Pin	Signal Name
1	GND
2	GND
3	CON_LBKLT_CTL
4	CON_LBKLT_EN
5	LCD_BLT_VCC
6	LCD_BLT_VCC
7	EDP_BKLEN
8	EDP_BKLT_CTRL

25 : eDP and LVDS Backlight Power Select (LCD_BLT_VCC) (BKT_PWR1)

1-2: LCD_BLT_VCC: +5V (Default)
2-3: LCD_BLT_VCC: +12V
4-5: LCD_BLT_VCC: DC_IN

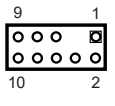
26 : CON_LBKLT_CTL Voltage Level (BLT_PWM2)

1-2: +3V (Default)
2-3: +5V



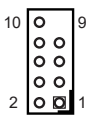
27 : SPI_TPM Header (SPI_TPM1)

Pin	Signal Name	Signal Name	Pin
1	TPM PWR	RST#	2
3		CS#	4
5	IRA	MOSI	6
7	MISO	GND	8
9	CLK	GND	10



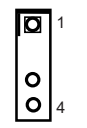
28 : USB 2.0 Headers (USB2_7_8, USB2_5_6)

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	USB_PWR	2
3	USB_D-	USB_D-	4
5	USB_D+	USB_D+	6
7	GND	GND	8
9		DUMMY	10



29 : SPDIF Header (SPDIF1)

Pin	Signal Name
1	+5V
2	
3	SPDIF OUT
4	GND

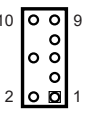


30 : 3W Audio AMP Output Wafer (SPEAKER1)

Pin	Signal Name
1	OUTLN
2	OUTLP
3	OUTRP
4	OUTRN

31 : Front Panel Audio Header (HD_AUDIO1)

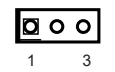
Pin	Signal Name	Signal Name	Pin
1	LIN1_L	GND	2
3	LIN1_R		4
5	HPOUT_R	LIN1_JD	6
7	GND		8
9	HPOUT_L	J_SENSE	10



32 : DC-In Jack (DC_IN1)
33 : Audio Jack: Pink - Mic In
34 : Audio Jack: Green - Line Out
35 : Top : HDMI Port (HDMI2)
Bottom : HDMI Port (HDMI1)

36 : USB2_5_6, USB_7_8 POWER (USB2_PWR1)

1-2 : +5V
2-3 : +5VSB (Default)



37 : USB8_S_M2E1

Pin	Signal Name
1	short USB2_7_8 Pin 4
2	short USB2_7_8 Pin 6

• Short Pin 1–2 to share USB2_7_8 signal (USB Port 8) with M2_E1.
• USB2_7_8 disabled if M.2 Key E USB2 is used.

38 : Top : USB 2.0 Port (USB2_4)
Bottom : USB 3.2 Gen2 Port (USB3_3)
39 : Top : USB 3.2 Gen2 Port (USB3_2)
Bottom : USB 3.2 Gen2 Port (USB3_1)
40 : RJ-45 LAN Port (LAN2)
41 : RJ-45 LAN Port (LAN1)

23 : Brightness Control Mode (BLT_PWM1)

1-2: From eDP PWM to CON_LBKLT_CTL
2-3: From LVDS PWM to CON_LBKLT_CTL (Default)

• Please set to 1-2 when adjusting brightness by Brightness Control bar under OS.
• Please set to 2-3 when adjusting brightness by BLT_VOL1.