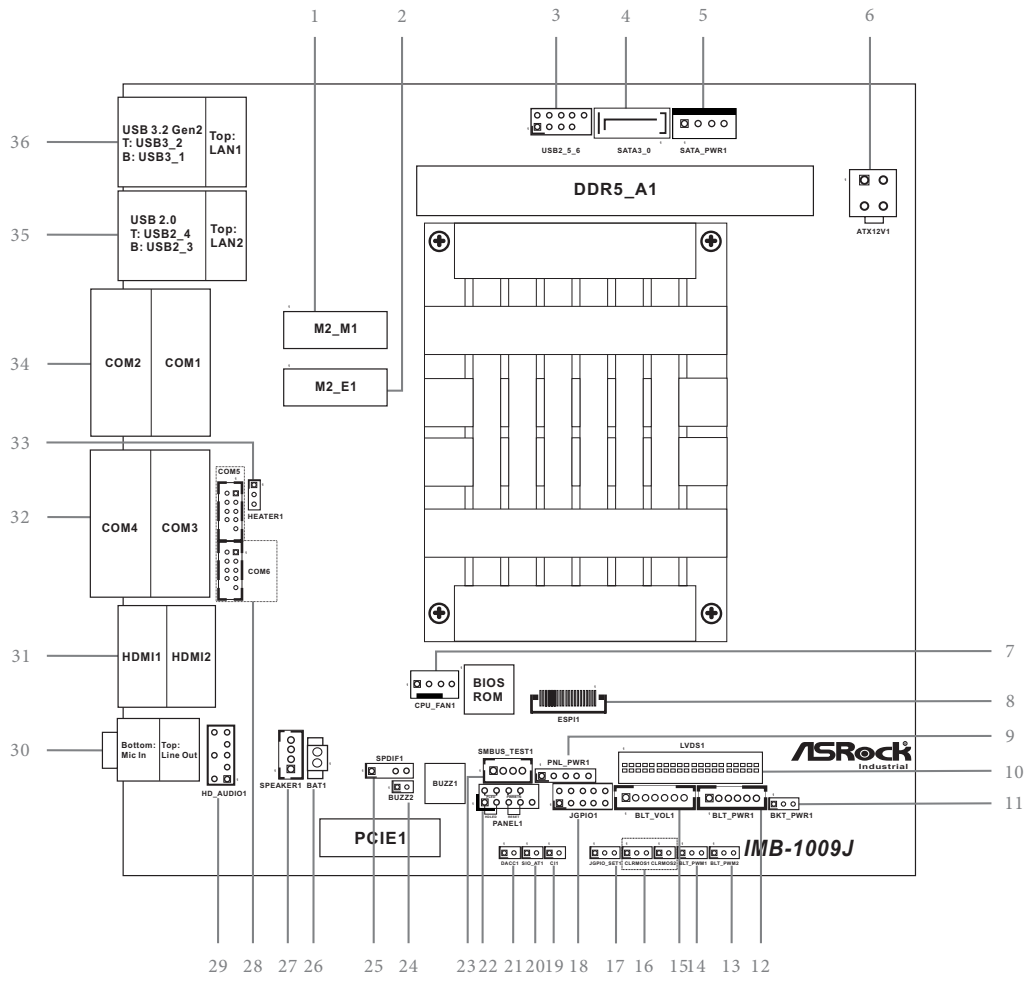
Jumpers and Headers Setting Guide

ASRock Industrial

IMB-1009J

Revision History

Date	Description
November 26, 2024	First Release
May 21, 2026	Second Release



1 : M.2 Key-M Socket (M2_M1)

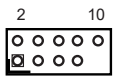
Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	NA	NA	6
7	NA	NA	8
9	GND	SATA_LED	10
11	NA	+3.3V	12
13	NA	+3.3V	14
15	GND	+3.3V	16
17	NA	+3.3V	18
19	NA	NA	20
21	GND	NA	22
23	NA	NA	24
25	NA	NA	26
27	GND	NA	28
29	NA	NA	30
31	NA	NA	32
33	GND	NA	34
35	NA	NA	36
37	NA	NA	38
39	GND	NA	40
41	PERn0/SATA-B+	NA	42
43	PERp0/SATA-B-	NA	44
45	GND	NA	46
47	PETn0/SATA-A-	NA	48
49	PETp0/SATA-A+	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

2 : M.2 Key-E Socket (M2_E1)

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	USB_D+	+3.3V	4
5	USB_D-	NA	6
7	GND	NA	8
9	CNV_WGR_D1-	CNV_RF_RESET	10
11	CNV_WGR_D1+	NA	12
13	GND	MODEM_CLKREQ	14
15	CNV_WGR_D0-	NA	16
17	CNV_WGR_D0+	GND	18
19	GND	NA	20
21	CNV_WGR_CLK-	CNV_BRI_RSP	22
23	CNV_WGR_CLK+		
33	GND	CNV_BGI_DT	32
35	PETp	CNV_RGI_RSP	34
37	PETn	CNV_BRI_DT	36
39	GND	NA	38
41	PERp	NA	40
43	PERn	NA	42
45	GND	NA	44
47	PEFCLKp	NA	46
49	PEFCLKn	NA	48
51	GND	SUSCLK	50
53	CLKREQ#	PERST0#	52
55	NA	W_DISABLE1#	54
57	GND	W_DISABLE2#	56
59	CNV_WT_D1-	SMB_DATA	58
61	CNV_WT_D1+	SMB_CLK	60
63	GND	NA	62
65	CNV_WT_D0-	NA	64
67	CNV_WT_D0+	NA	66
69	GND	NA	68
71	CNV_WT_CLK-	NA	70
73	CNV_WT_CLK+	+3.3V	72
75	GND	+3.3V	74

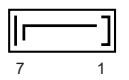
3 : USB 2.0 Header (USB2_5_6)

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	USB_PWR	2
3	USB_D-	USB_D-	4
5	USB_D+	USB_D+	6
7	GND	GND	8
9		DUMMY	10



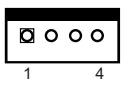
4 : SATA3 Connector (SATA3_0)

Pin	Signal Name
1	GND
2	SATA-A+
3	SATA-A-
4	GND
5	SATA-B-
6	SATA-B+
7	GND



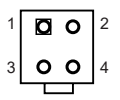
5 : SATA Power Output Connector (SATA_PWR1)

Pin	Signal Name
1	+5V
2	GND
3	GND
4	+12V



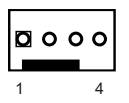
6 : 4-pin Power Connector (ATX12V1)

1-2: GND
3-4: DC Input (12V only)



7 : CPU FAN Connector (+12V) (CPU_FAN1)

Pin	Signal Name
1	GND
2	+12V
3	CPU_FAN_SPEED
4	CPU_SPEED_CONTROL

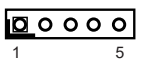


8 : ESPI Header (ESPI1)

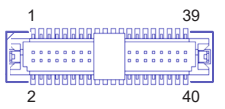
Pin	Signal Name
1	GND
2	ESPI_CLK
3	GND
4	ESPI_CS#
5	ESPI_RESET#
6	GND
7	+3V
8	ESPI_CS#1
9	PLTRST#
10	COM_RST#
11	ESPI_IO0
12	ESPI_IO1
13	ESPI_IO2
14	ESPI_IO3
15	ALERT#1
16	+3VSB
17	Internal Use
18	+5VSB
19	ESPI_ALERT#
20	GND

9 : eDP and LVDS Panel Power Select (LCD_VCC) (PNL_PWR1)

1-2: LCD_VCC: +3V (Default)
2-3: LCD_VCC: +5V
4-5: LCD_VCC: +12V



10 : LVDS Panel Connector (LVDS1)



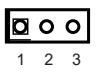
・eDP pin definition (switch by BIOS):

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	+3.3V	NA	4
5	NA	LVDS_A_DATA0#	6
7	LVDS_A_DATA0	GND	8
9	LVDS_A_DATA1#	LVDS_A_DATA1	10
11	GND	LVDS_A_DATA2#	12
13	LVDS_A_DATA2	GND	14
15	LVDS_A_DATA3#	LVDS_A_DATA3	16
17	GND	LVDS_A_CLK#	18
19	LVDS_A_CLK	GND	20
21	LVDS_B_DATA0#	LVDS_B_DATA0	22
23	GND	LVDS_B_DATA1#	24
25	LVDS_B_DATA1	GND	26
27	LVDS_B_DATA2#	LVDS_B_DATA2	28
29	DPLVDD_EN	LVDS_B_DATA3#	30
31	LVDS_B_DATA3	GND	32
33	LVDS_B_CLK#	LVDS_B_CLK	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	NA	NA	4
5	NA	NA	6
7	NA	GND	8
9	EDP_TX1#	EDP_TX1	10
11	GND	EDP_TX0#	12
13	EDP_TX0	GND	14
15	NA	NA	16
17	GND	EDP_AUXN	18
19	EDP_AUXP	GND	20
21	NA	NA	22
23	GND	NA	24
25	NA	GND	26
27	NA	NA	28
29	DPLVDD_EN	NA	30
31	NA	GND	32
33	NA	NA	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40

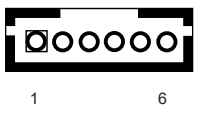
11 : eDP and LVDS Backlight Power Select (LCD_BLT_VCC) (BKT_PWR1)

1-2: LCD_BLT_VCC: +5V (Default)
2-3: LCD_BLT_VCC: +12V



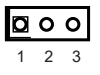
12 : Backlight Power Connector (BLT_PWR1)

Pin	Signal Name
1	GND
2	GND
3	CON_LBKLT_CTL
4	CON_LBKLT_EN
5	LCD_BLT_VCC
6	LCD_BLT_VCC



13 : CON_LBKLT_CTL Voltage Level (BLT_PWM2)

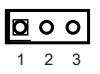
1-2: +3V (Default)
2-3: +5V

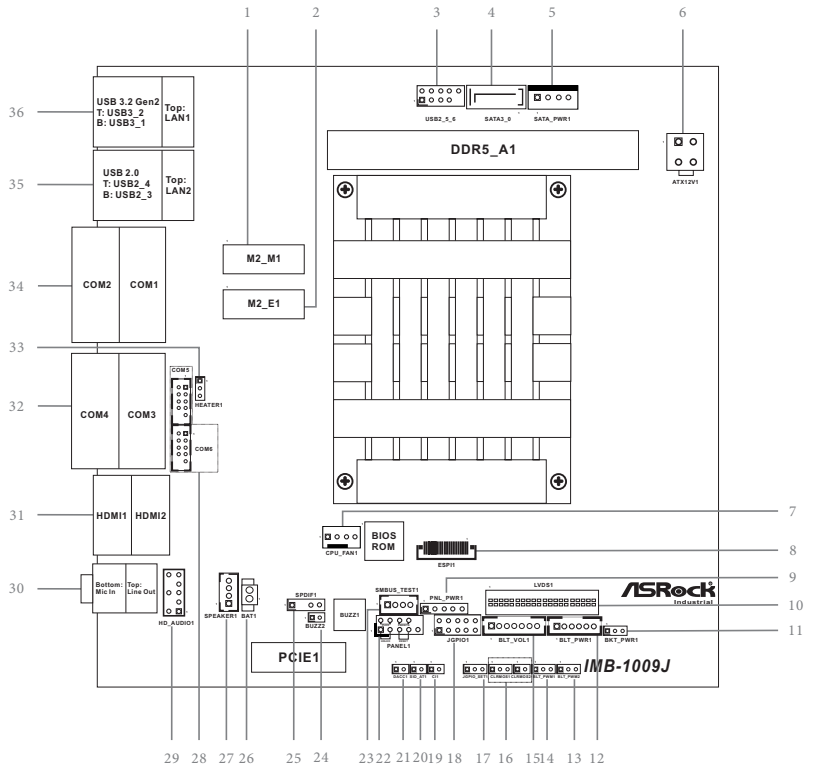


14 : Brightness Control Mode (BLT_PWM1)

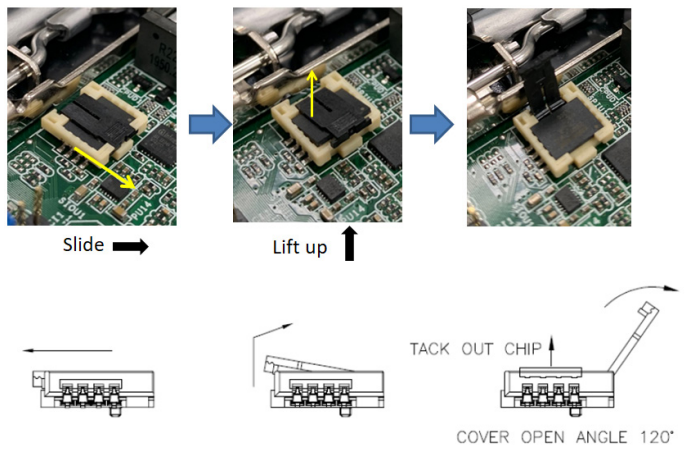
1-2: From eDP PWM to CON_LBKLT_CTL
2-3: From LVDS PWM to CON_LBKLT_CTL (Default)

• Please set to 1-2 when adjusting brightness by Brightness Control bar under OS.
• Please set to 2-3 when adjusting brightness by BLT_VOL1.

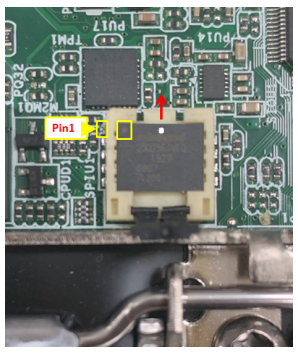




Installation of ROM Socket



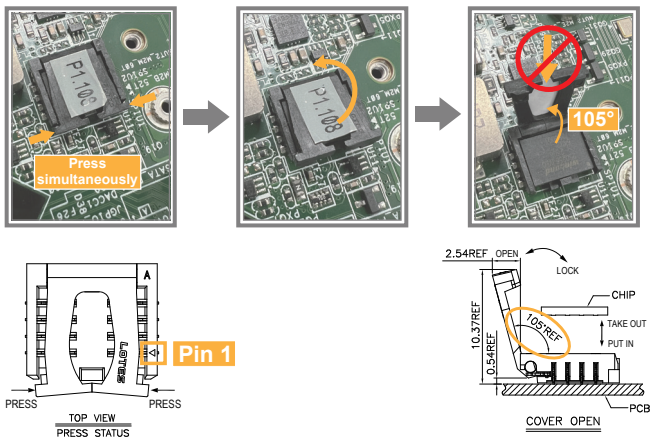
- Do not apply force to the actuator cover after ic inserted.
- Do not apply force to actuator cover when it is opening over 120 degree, Otherwise, the actuator cover may be broken.



- The yellow dot (Pin1) on the ROM must be installed at pin1 position of the socket (white arrow area).
- Make sure the white dot on the ROM is installed outwards of the socket.
- For further details of how to install ROM, please refer to ASRI website.

Warning: If the installation does not follow as the picture, then it may cause severe damage to chipset & MB.

Installation of LOTES ROM Socket



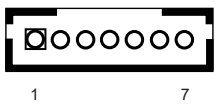
- Do not press one side of the actuator cover at a time. Always apply even and simultaneous force to both sides to avoid damage.
- Do not apply force to the actuator cover after the IC is inserted, especially when it is fully opened at 105 degrees. Pressing vertically at this angle may cause the cover to break.

- The white dot (Pin 1) on the ROM must align with the Pin 1 position of the socket (white arrow area).
- Ensure the white dot on the ROM is facing outward from the socket.

Warning: Incorrect installation may damage the chipset and motherboard. Refer to the picture for proper orientation.

15 : Backlight Volume Control (BLT_VOL1)

Pin	Signal Name
1	GPIO_VOL_UP
2	GPIO_VOL_DW
3	PWRDN
4	BLT_UP
5	BLT_DW
6	GND
7	GND



16 : Clear CMOS Jumpers

CLRMOS1:
1-2: Normal (Default)
2-3: Clear CMOS

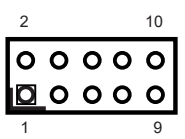
CLRMOS2:
Open: Normal (Default)
Short: Auto Clear CMOS When AC Power On

17 : Digital Input / Output Default Value Setting (JGPIO_SET1)

(only setting for GPP_A14~17)
1-2: Pull-High (Default)
2-3: Pull-Low

18 : Digital Input/Output Pin Header (JGPIO1)

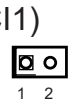
Pin	Signal Name	Signal Name	Pin
1	GPP_A14	GPP_B15	2
3	GPP_A15	GPP_E1	4
5	GPP_A16	GPP_E2	6
7	GPP_A17	GPP_E13	8
9	+3V	GND	10



Parameter	Range
GPIO input Low voltage	Max: 0.9V
GPIO input High voltage	Low: 2.5V
GPIO output Low voltage	Max: 0.45V
GPIO output High voltage	Low: 2.85V
Note: Max. load per GPI/O pin: 3mA Current Max. 1A per power pin.	

19 : Chassis Intrusion Header (CI1)

Open: Normal (Default)
Short: Active Case Open



20 : SIO_AT1

Open: ATX Mode (Default)
Short: AT Mode

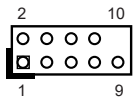
21 : DACC1

Open: Normal
Short: Auto Clear CMOS (Default)

- Note: Auto clear CMOS when system boot improperly.

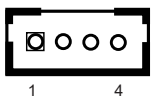
22 : System Panel Header (PANEL1)

Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	GND		10



23 : SMBUS_TEST1

Pin	Signal Name
1	GPIO
2	SMB_CLK
3	SMB_DATA
4	GND

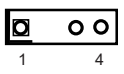


24 : Buzzer Header (BUZZ2)

Pin	Signal Name
1	BUZZ+
2	BUZZ-

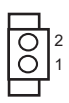
25 : SPDIF Header (SPDIF1)

Pin	Signal Name
1	+5V
2	
3	SPDIF OUT
4	GND



26 : Battery Connector (BAT1)

Pin	Signal Name
1	+BAT
2	GND

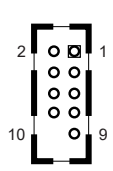


27 : 3W Audio AMP Output Wafer (SPEAKER1)

Pin	Signal Name
1	OUTLN
2	OUTLP
3	OUTRP
4	OUTRN

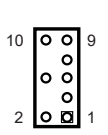
28 : Internal COM Port Headers (COM5, 6) (RS232)

Pin	Signal Name	Signal Name	Pin
1	DDCD#	RRXD	2
3	TTXD	DDTR#	4
5	GND	DDSR#	6
7	RRTS#	CCTS#	8
9	NA		10



29 : Front Panel Audio Header (HD_AUDIO1)

Pin	Signal Name	Signal Name	Pin
1	MIC2_L	GND	2
3	MIC2_R		4
5	OUT2_R	MIC_RET	6
7	J_SENSE		8
9	OUT2_L	OUT_RET	10



30 : Audio Jacks

Top : Green - Line Out
Bottom : Pink - Mic In

31 : Top : HDMI Port (HDMI2)

Bottom : HDMI Port (HDMI1)

32 : Top : COM Port (COM3) (RS232)

Bottom : COM Port (COM4) (RS232)

33 : Heater Header (HEATER1)

Pin	Signal Name
1	Heater PWR
2	GND
3	NCT

34 : Top : COM Port (COM1) (RS232/422/485)*

Bottom : COM Port (COM2) (RS232)

* This motherboard supports RS232/422/485 on COM1 port. Please refer to the table below for the pin definition. In addition, COM1 port (RS232/422/485) can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

COM1 Port Pin Definition

Pin	RS232	RS422	RS485
1	DCD	TX-	RTX-
2	RXD	TX+	RTX+
3	TXD	RX+	N/A
4	DTR	RX-	N/A
5	GND	GND	GND
6	DSR	N/A	N/A
7	RTS	N/A	N/A
8	CTS	N/A	N/A
9	N/A	N/A	N/A
10	N/A	N/A	N/A

35 : Top : RJ45 LAN Port (LAN2)

Middle : USB 2.0 Port (USB2_4)
Bottom : USB 2.0 Port (USB2_3)

36 : Top : RJ45 LAN Port (LAN1)

Middle : USB 3.2 Gen2 Port (USB3_2)
Bottom : USB 3.2 Gen2 Port (USB3_1)